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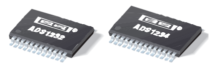


SBAS350C – JUNE 2005 – REVISED JUNE 2006

24-Bit Analog-to-Digital Converter For Bridge Sensor

FEATURES

- **Complete Front-End for Bridge Sensor**
- **Up to 23.5 Effective Bits**
- **Onboard, Low-Noise PGA**
- **RMS Noise:**
  17nV at 10SPS (PGA = 128)
  44nV at 80SPS (PGA = 128)
- **19.2-Bit Noise-Free Resolution at Gain = 64**
- **Over 100dB Simultaneous 50Hz and 60Hz Rejection**
- **Flexible Clocking:**
  Low-Drift Onboard Oscillator (±3%)
  Optional External Crystal
- **Selectable Gains of 1, 2, 64, and 128**
- **Easy Ratiometric Measurements–**
  External Voltage Reference up to 5V
- **Selectable 10SPS or 80SPS Data Rates**
- **Two-Channel Differential Input with Built-In Temperature Sensor (ADS1232)**
- **Four-Channel Differential Input (ADS1234)**
- **Simple Serial Digital Interface**
- **Supply Range: 2.7V to 5.3V**
- **–40°C to +105°C Temperature Range**

APPLICATIONS

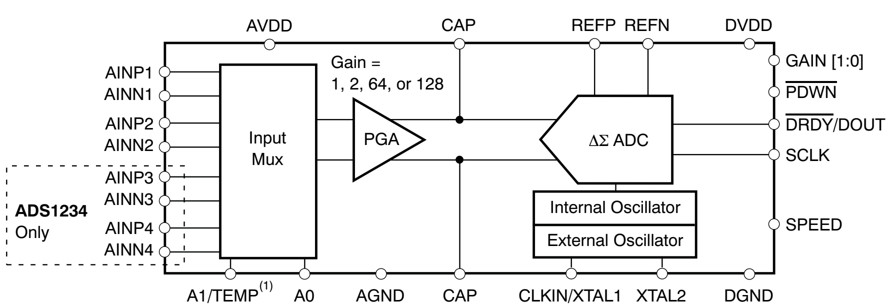
- **Weigh Scales**
- **Strain Gauges**
- **Pressure Sensors**
- **Industrial Process Control**

DESCRIPTION

The ADS1232 and ADS1234 are precision 24-bit analog-to-digital converters (ADCs). With an onboard, low-noise programmable gain amplifier (PGA), precision delta-sigma ADC and internal oscillator, the ADS1232/4 provide a complete front-end solution for bridge sensor applications including weigh scales, strain gauges and pressure sensors.

The input multiplexer accepts either two (ADS1232) or four (ADS1234) differential inputs. The ADS1232 also includes an onboard temperature sensor to monitor ambient temperature. The onboard, low-noise PGA has a selectable gain of 1, 2, 64, or 128 supporting a full-scale differential input of ±2.5V, ±1.25V, ±39mV, or ±19.5mV. The delta-sigma ADC has 23.5-bit effective resolution and is comprised of a 3rd-order modulator and 4th-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1232/4 can be clocked externally using an oscillator or a crystal. There is also an internal oscillator available that requires no external components. Offset calibration is performed on-demand and the ADS1232/4 can be put in a low-power standby mode or shut off completely in power-down mode. All of the features of the ADS1232/4 are operated through simple pin-driven control. There are no digital registers to program in order to simplify software development. Data is output over an easily-isolated serial interface that connects directly to the MSP430 and other microcontrollers.

The ADS1232 is available in a TSSOP-24 package and the ADS1234 is in a TSSOP-28. Both are fully specified from -40°C to +105°C.



NOTE: (1) A1 for ADS1234, TEMP for ADS1232.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	ADS1232, ADS1234	UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +6	V
AGND to DGND	–0.3 to +0.3	V
Input Current	100, Momentary	mA
Input Current	10, Continuous	mA
Analog Input Voltage to AGND	–0.3 to AVDD + 0.3	V
Digital Input Voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +105	°C
Storage Temperature Range	–60 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = –40°C to +105°C, AVDD = DVDD = VREFP = +5V, and VREFN = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1232, ADS1234 MIN	TYP	MAX	UNIT
Analog Inputs					
Full-Scale Input Voltage (AINP – AINN)			±0.5V_{REF}/Gain		V
Common-Mode Input Range	AINxP or AINxN with respect to GND, Gain = 1, 2	AGND – 0.1		AVDD + 0.1	V
	Gain = 64, 128	AGND + 1.5V		AVDD – 1.5V	V
Differential Input Current	Gain = 1		±3		nA
	Gain = 2		±6		nA
	Gain = 64, 128		±3.5		nA
System Performance					
Resolution	No Missing Codes	24			Bits
Data Rate	Internal Oscillator, SPEED = High	78	80	82.4	SPS
	Internal Oscillator, SPEED = Low	9.75	10	10.3	SPS
	External Oscillator, SPEED = High		f_{CLK}/61,440		SPS
	External Oscillator, SPEED = Low		f_{CLK}/491,520		SPS
Digital Filter Settling Time	Full Settling		4		Conversions
Integral Nonlinearity (INL)	Differential Input, End-Point Fit Gain = 1, 2		±0.0002	±0.001	% of FSR[1]
	Differential Input, End-Point Fit Gain = 64, 128		±0.0004		% of FSR
Input Offset Error[2]	Gain = 1		±0.2	±5	ppm of FS
	Gain = 128		±0.02	±1	ppm of FS
Input Offset Drift	Gain = 1		±0.3		µV/°C
	Gain = 128		±10		nV/°C
Gain Error[3]	Gain = 1		±0.001	±0.02	%
	Gain = 128		±0.01	±0.1	%
Gain Drift	Gain = 1		±0.2		ppm/°C
	Gain = 128		±2.5		ppm/°C
Normal-Mode Rejection[4]	Internal Oscillator, f_{DATA} = 10SPS f_{IN} = 50Hz or 60Hz, ±1Hz	100	110		dB
	External Oscillator, f_{DATA} = 10SPS f_{IN} = 50Hz or 60Hz, ±1Hz	120	130		dB
Common-Mode Rejection	at DC, Gain = 1, ΔVDD = 1V	95	110		dB
	at DC, Gain = 128, ΔVDD = 0.1V	95	110		dB
Input-Referred Noise			See Noise Performance Tables		
Power-Supply Rejection	at DC, Gain = 1, ΔVDD = 1V	100	120		dB
	at DC, Gain = 128, ΔVDD = 0.1V	100	120		dB
Voltage Reference Input					
Voltage Reference Input (V_{REF})	V_{REF} = VREFP – VREFN	1.5	AVDD	AVDD + 0.1V	V
Negative Reference Input (VREFN)		AGND – 0.1		VREFP – 1.5	V
Positive Reference Input (VREFP)		VREFN + 1.5		AVDD + 0.1	V
Voltage Reference Input Current			10		nA

(1) FSR = full-scale range = V_{REF}/Gain.
(2) Offset calibration can minimize these errors to the level of noise at any temperature.
(3) Gain errors are calibrated at the factory (AVDD = +5V, all gains, T_A = +25°C).
(4) Specification is assured by the combination of design and final production test.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –40°C to +105°C, AVDD = DVDD = VREFP = +5V, and VREFN = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1232, ADS1234 MIN	TYP	MAX	UNIT
Digital					
Logic Levels					
V_{IH}	All digital inputs except CLKIN/XTAL1	0.7 DVDD		DVDD + 0.1	V
	CLKIN/XTAL1	0.7 DVDD		5.1	V
V_{IL}		DGND		0.2 DVDD	V
V_{OH}	I_{OH} = 1mA	DVDD – 0.4			V
V_{OL}	I_{OL} = 1mA			0.2 DVDD	V
Input Leakage	0 < V_{IN} < DVDD			±10	µA
External Clock Input Frequency (f_{CLKIN})		0.2	4.9152	8	MHz
Serial Clock Input Frequency (f_{SCLK})				5	MHz
Power Supply					
Power-Supply Voltage (AVDD, DVDD)		2.7		5.3	V
Analog Supply Current	Normal Mode, AVDD = 3V, Gain = 1, 2		600	1300	µA
	Normal Mode, AVDD = 3V, Gain = 64, 128		1350	2500	µA
	Normal Mode, AVDD = 5V, Gain = 1, 2		650	1300	µA
	Normal Mode, AVDD = 5V, Gain = 64, 128		1350	2500	µA
	Standby Mode		0.1	1	µA
	Power-Down		0.1	1	µA
Digital Supply Current	Normal Mode, DVDD = 3V, Gain = 1, 2		60	95	µA
	Normal Mode, DVDD = 3V, Gain = 64, 128		75	120	µA
	Normal Mode, DVDD = 5V, Gain = 1, 2		95	130	µA
	Normal mode, DVDD = 5V, Gain = 64, 128		75	120	µA
	Standby Mode, SCLK = High, DVDD = 3V		45	80	µA
	Standby Mode, SCLK = High, DVDD = 5V		65	80	µA
	Power-Down		0.2	1.3	µA
Power Dissipation, Total	Normal Mode, AVDD = DVDD = 3V, Gain = 1, 2		2	4.2	mW
	Normal Mode, AVDD = DVDD = 5V, Gain = 1, 2		3.7	7.2	mW
	Normal Mode, AVDD = DVDD = 3V, Gain = 64, 128		4.3	7.9	mW
	Normal Mode, AVDD = DVDD = 5V, Gain = 64, 128		7.1	13.1	mW
	Standby Mode, AVDD = DVDD = 5V		0.3	0.4	mW

NOISE PERFORMANCE

The ADS1232/4 offer outstanding noise performance that can be optimized for a given full-scale range using the on-chip programmable gain amplifier. Table 1 through Table 4 summarize the typical noise performance with inputs shorted externally for different gains, data rates, and voltage reference values.

The RMS and Peak-to-Peak noise are referred to the input. The Effective Number of Bits (ENOB) is defined as:

- ENOB = ln (FSR/RMS noise)/ln(2)

The Noise-Free Bits are defined as:

- Noise-Free Bits = ln (FSR/Peak-to-Peak Noise)/ln(2)

Where FSR (Full-Scale Range) = V_{REF}/Gain

Table 1. AVDD = 5V, V_{REF} = 5V, Data Rate = 10SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	ENOB (RMS)	NOISE-FREE BITS
1	420nV	1.79µV	23.5	21.4
2	270nV	900nV	23.1	21.4
64	19nV	125nV	22.0	19.2
128	17nV	110nV	21.1	18.4

(1) Peak-to-peak noise data is based on direct measurement.

Table 2. AVDD = 5V, V_{REF} = 5V, Data Rate = 80SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	ENOB (RMS)	NOISE-FREE BITS
1	1.36µV	8.3µV	21.8	19.2
2	850nV	5.5µV	21.5	18.8
64	48nV	307nV	20.6	18
128	44nV	247nV	19.7	17.2

(1) Peak-to-peak noise data is based on direct measurement.

Table 3. AVDD = 3V, V_{REF} = 3V, Data Rate = 10SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	ENOB (RMS)	NOISE-FREE BITS
1	450nV	2.8µV	22.6	20
2	325nV	1.8µV	22.1	19.7
64	20nV	130nV	21.2	18.5
128	18nV	115nV	20.3	17.6

(1) Peak-to-peak noise data is based on direct measurement.

Table 4. AVDD = 3V, V_{REF} = 3V, Data Rate = 80SPS

GAIN	RMS NOISE	PEAK-TO-PEAK NOISE(1)	ENOB (RMS)	NOISE-FREE BITS
1	2.2µV	12µV	20.4	17.9
2	1.2µV	6.8µV	20.2	17.8
64	54nV	340nV	19.7	17.1
128	48nV	254nV	18.9	16.5

(1) Peak-to-peak noise data is based on direct measurement of 1024 samples.

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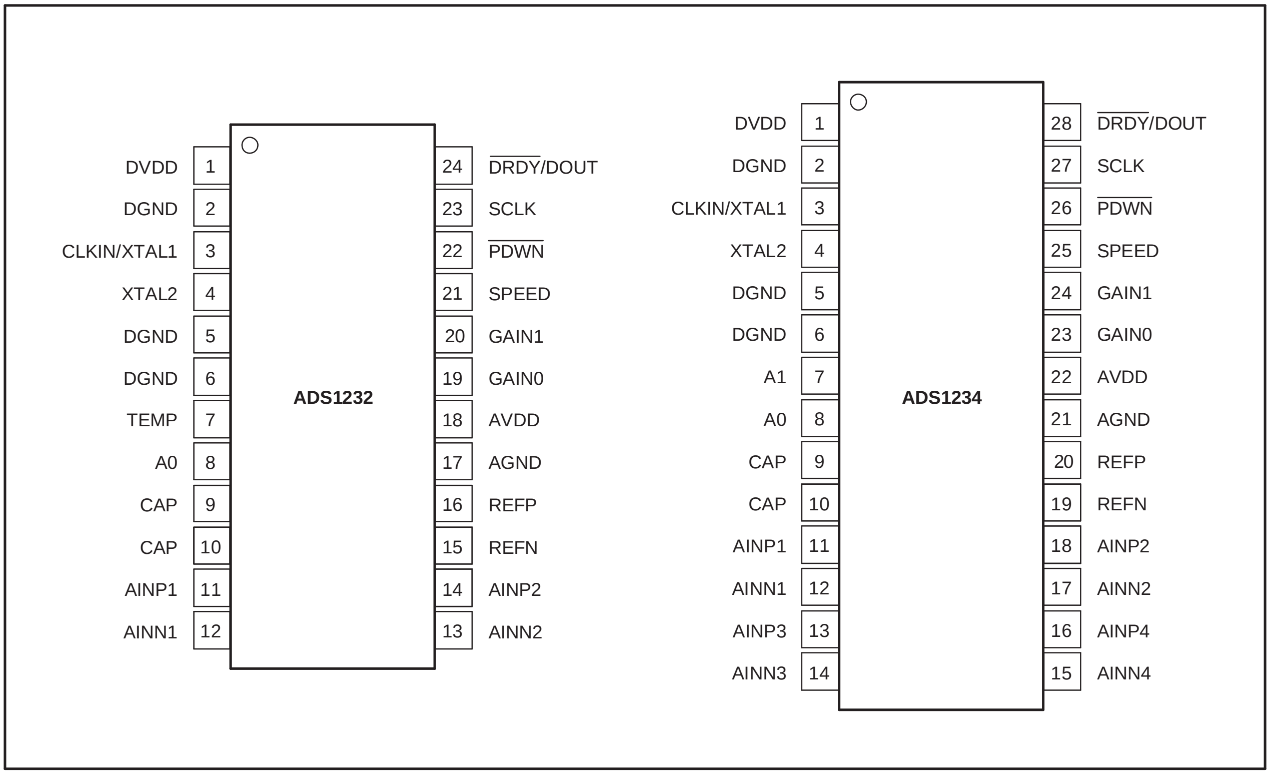
PIN CONFIGURATION



PIN CONFIGURATION (continued)

PIN DESCRIPTIONS

NAME	TERMINAL		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
	ADS1232	ADS1234		
DVDD	1	1	Digital	Digital Power Supply: 2.7V to 5.3V
DGND	2	2	Digital	Digital Ground
CLKIN/ XTAL1	3	3	Digital/Digital Input	External Clock Input: typically 4.9152MHz. Tie low to activate internal oscillator. Can also use external crystal across CLKIN/XTAL1 and XTAL2 pins. See text for more details.
XTAL2	4	4	Digital	External crystal connection
DGND	5	5	Digital	Digital Ground
DGND	6	6	Digital	Digital Ground
TEMP	7	–	Digital Input	Onboard Temperature Diode Enable
A1 A0	– 8	7 8	Digital Input	Input Mux Select Input pin (MSB) Input Mux Select Input pin (LSB): **A1 A0 Channel** 0 0 AIN1 0 1 AIN2 1 0 AIN3 1 1 AIN4
CAP	9	9	Analog	Gain Amp Bypass Capacitor Connection
CAP	10	10	Analog	Gain Amp Bypass Capacitor Connection
AINP1	11	11	Analog Input	Positive Analog Input Channel 1
AINN1	12	12	Analog Input	Negative Analog Input Channel 1
AINP3	–	13	Analog Input	Positive Analog Input Channel 3
AINN3	–	14	Analog Input	Negative Analog Input Channel 3
AINN4	–	15	Analog Input	Negative Analog Input Channel 4
AINP4	–	16	Analog Input	Positive Analog Input Channel 4
AINN2	13	17	Analog Input	Negative Analog Input Channel 2
AINP2	14	18	Analog Input	Positive Analog Input Channel 2
REFN	15	19	Analog Input	Negative Reference Input
REFP	16	20	Analog Input	Positive Reference Input
AGND	17	21	Analog	Analog Ground
AVDD	18	22	Analog	Analog Power Supply, 2.7V to 5.3V
GAIN0 GAIN1	19 20	23 24	Digital Input	Gain Select **GAIN1 GAIN0 GAIN** 0 0 1 0 1 2 1 0 64 1 1 128
SPEED	21	25	Digital Input	Data Rate Select: **SPEED DATA RATE** 0 10SPS 1 80SPS
$\overline{\text{PDWN}}$	22	26	Digital Input	Power-Down: Holding this pin low powers down the entire converter and resets the ADC.
SCLK	23	27	Digital Input	Serial Clock: Clock out data on the rising edge. Also used to initiate Offset Calibration and Sleep modes. See text for more details.
$\overline{\text{DRDY}}$/ DOUT	24	28	Digital Output	Dual-Purpose Output: Data Ready: Indicates valid data by going low. Data Output: Outputs data, MSB first, on the first rising edge of SCLK.

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = DVDD = VREFP = 5V, and VREFN = AGND, unless otherwise noted.

NOISE PLOT

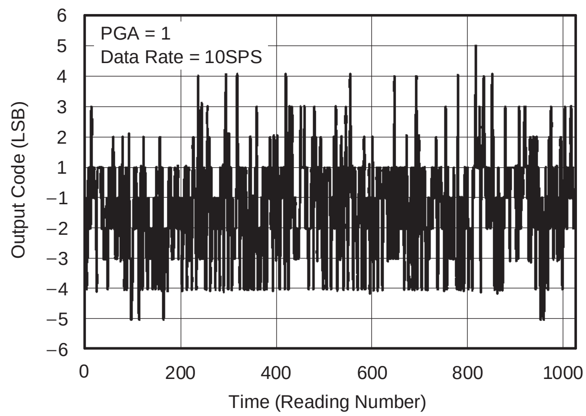


Figure 1.

NOISE PLOT

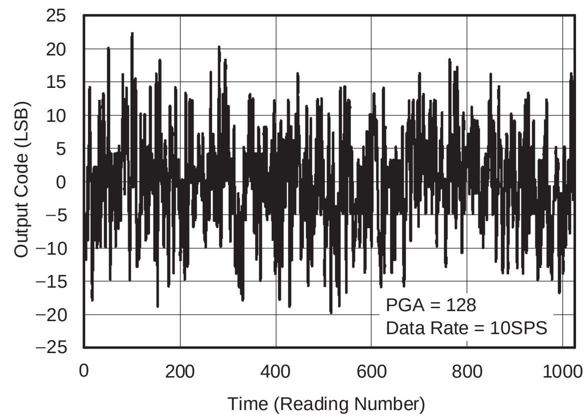


Figure 2.

NOISE HISTOGRAM

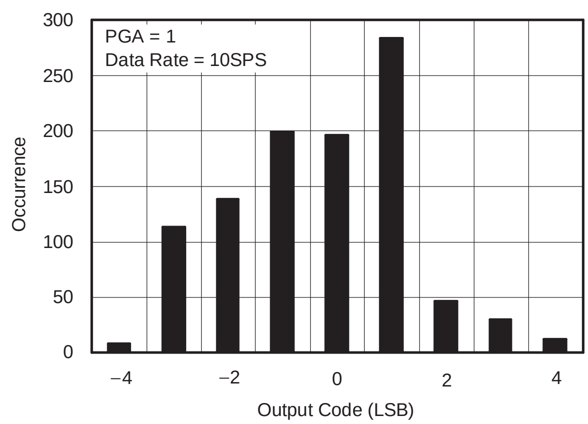


Figure 3.

NOISE HISTOGRAM

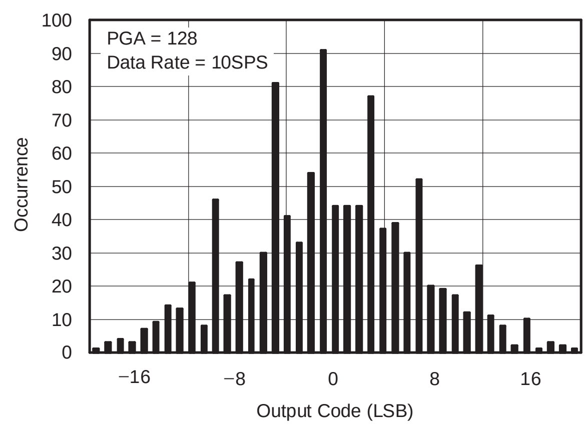


Figure 4.

NOISE PLOT

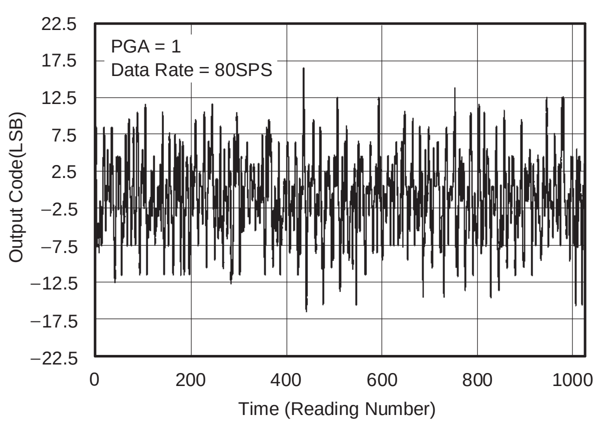


Figure 5.

NOISE PLOT

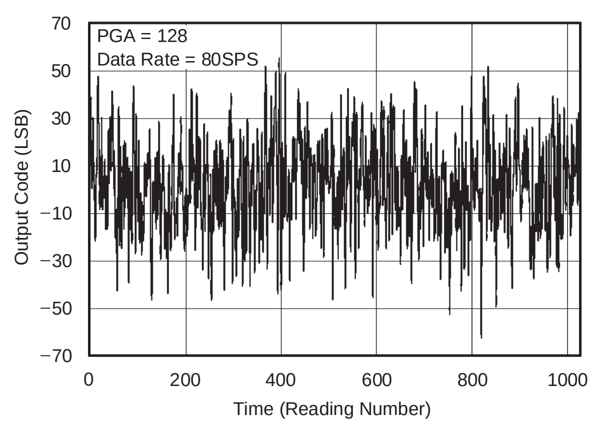


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = DVDD = VREFP = 5V, and VREFN = AGND, unless otherwise noted.

NOISE HISTOGRAM

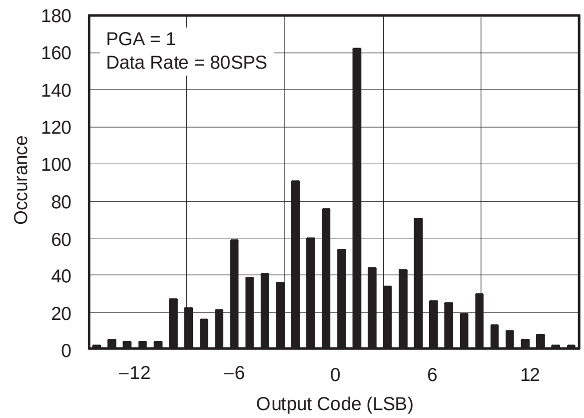


Figure 7.

NOISE HISTOGRAM

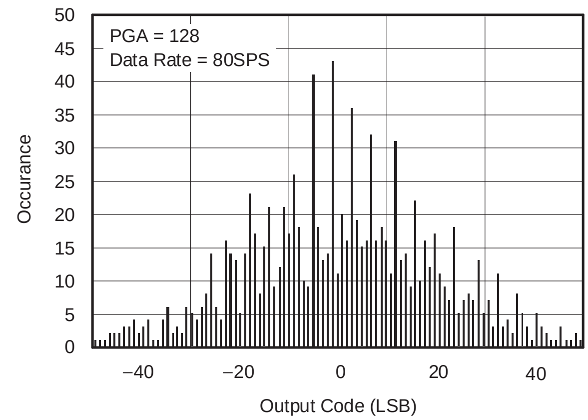


Figure 8.

OFFSET vs TEMPERATURE

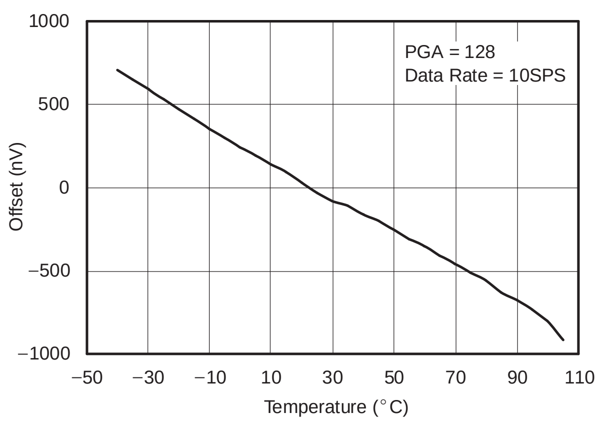


Figure 9.

GAIN ERROR vs TEMPERATURE

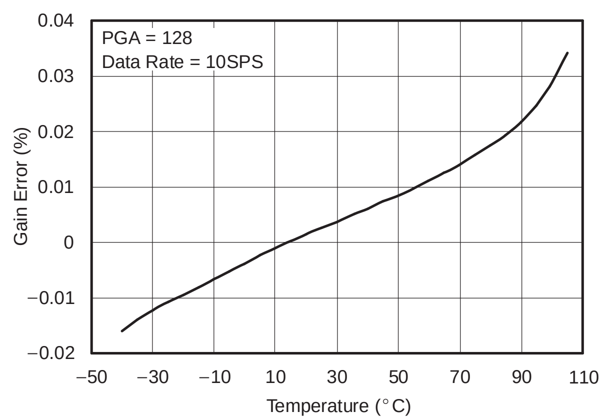


Figure 10.

NOISE vs INPUT SIGNAL

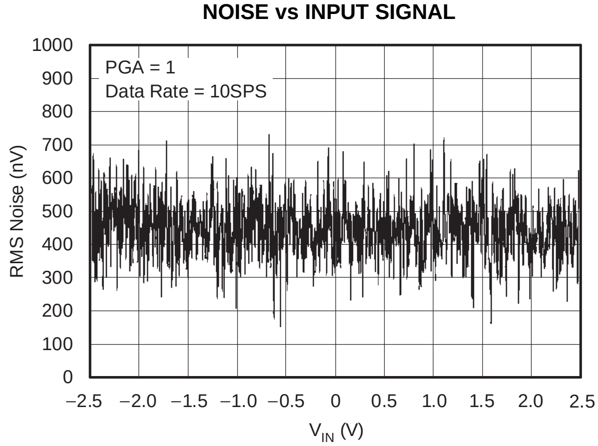


Figure 11.

NOISE vs INPUT SIGNAL

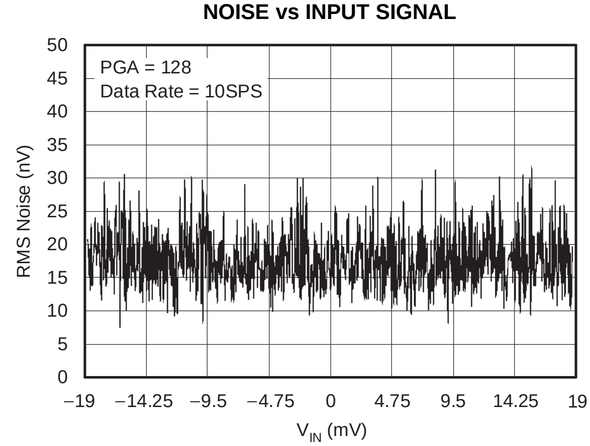


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = DVDD = VREFP = 5V, and VREFN = AGND, unless otherwise noted.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

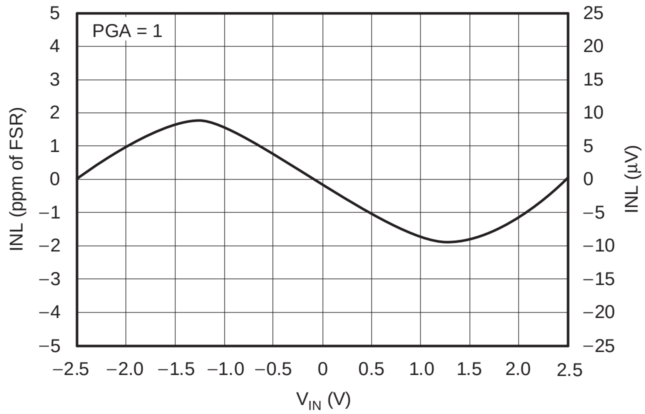


Figure 13.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

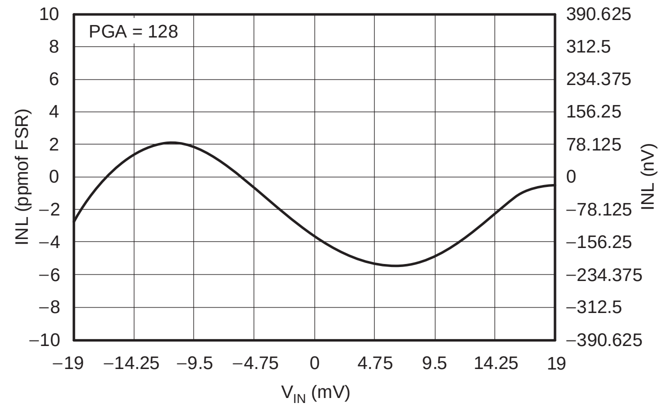


Figure 14.

ANALOG CURRENT vs TEMPERATURE

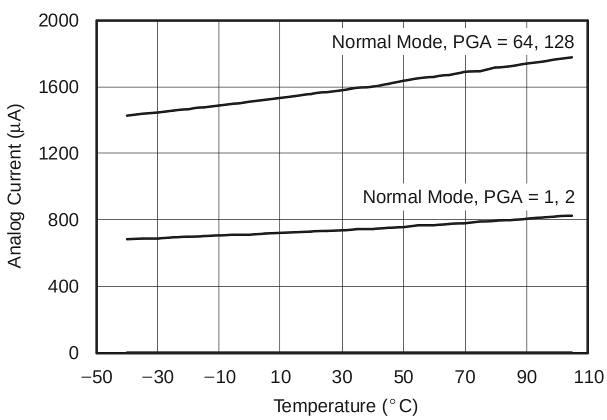


Figure 15.

DIGITAL CURRENT vs TEMPERATURE

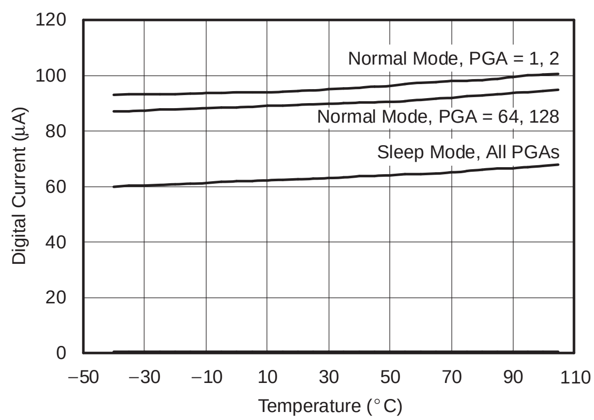


Figure 16.

DATA RATE vs TEMPERATURE

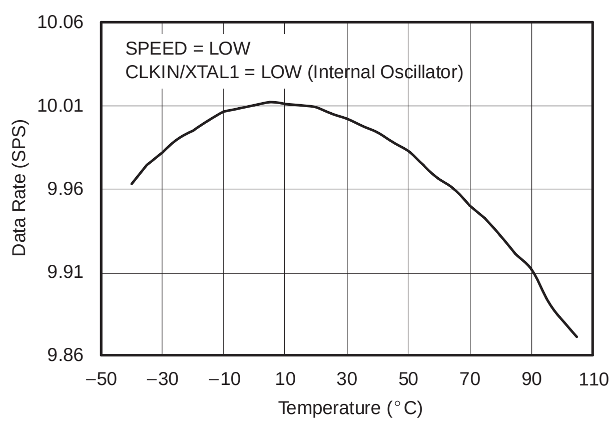


Figure 17.

OVERVIEW

The ADS1232 and ADS1234 are highly integrated, 24-bit ADCs that include an input multiplexer, low-noise PGA, third-order delta-sigma (ΔΣ) modulator, and fourth-order digital filter. With input-referred RMS noise down to 17nV, the ADS1232/4 are ideally suited for measuring the very low signals produced by bridge sensors in applications such as weigh scales, strain gauges, and pressure sensors.

Clocking can be supplied by an external oscillator, an external crystal, or by a precision internal oscillator. Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1232/4 are easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

ANALOG INPUTS (AINPx, AINNx)

The input signal to be measured is applied to the input pins AINPx and AINNx. The positive internal input is generalized as AINP, and the negative internal input generalized as AINN. The signal is selected through the input mux, which is controlled by pins A0 and A1 (ADS1234 only), as shown in Table 5. For the ADS1232, the A1 pin is replaced by the TEMP pin to activate the onboard diodes (see the *Temperature Sensor* section for more details). The ADS1232/4 accept differential input signals, but can also measure unipolar signals. When measuring unipolar (or single-ended signals) with respect to ground, connect the negative input (AINNx) to ground and connect the input signal to the positive input (AINPx). Note that when the ADS1232/4 are configured this way, only half of the converter full-scale range is used, since only positive digital output codes are produced.

Table 5. Input Channel Selection with A0 and A1 (ADS1234 only)

MUX PINS		SELECTED ANALOG INPUTS	
A1	A0	POSITIVE INPUT	NEGATIVE INPUT
0	0	AINP1	AINN1
0	1	AINP2	AINN2
1	0	AINP3	AINN3
1	1	AINP4	AINN3

TEMPERATURE SENSOR (ADS1232 only)

On-chip diodes provide temperature-sensing capability. By setting the TEMP pin high, the selected analog inputs are disconnected and the inputs to the ADC are connected to the anodes of two diodes scaled to 1x and 80x in current and size, as shown in Figure 18. By measuring the difference in voltage of these diodes, temperature changes can be inferred from a baseline temperature. Typically, the difference in diode voltage is 111.7mV at 25°C with a temperature coefficient of 379µV/°C. With PGA = 1 and 2, the difference voltage output from the PGA will be 111.7mV and 323.4mV, respectively. With PGA = 64 and 128, it is impossible to use the temperature sensor function. A similar structure is used in the MSC1210 for temperature measurement. For more information, see TI application report SBAA100, *Using the MSC121x as a High-Precision Intelligent Temperature Sensor*, available for download at www.ti.com.

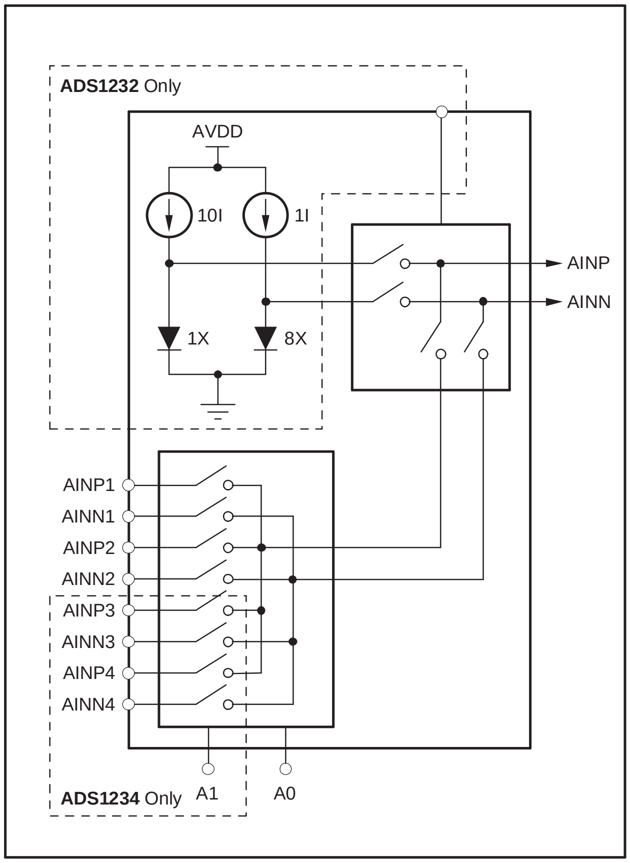


Figure 18. Measurement of the Temperature Sensor in the Input Multiplexer

LOW-NOISE PGA

The ADS1232/4 features a low-drift, low-noise PGA that provides a complete front-end solution for bridge sensors. A simplified diagram of the PGA is shown in Figure 19. It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately-matched resistors (R_1, R_{F1}, and R_{F2}), which construct a differential front-end stage with a gain of 64, followed by gain stage A3. The PGA inputs are equipped with an EMI filter, as shown in Figure 19. The cut-off frequency of the EMI filter is 19.6MHz. If the PGA is set to 1 or 2, the gain-of-64 stage is bypassed and shut down to save power. With the combination of both gain stages, the PGA can be set to 64 or 128. The PGA of the ADS1232/4 can be set to 1, 2, 64, or 128 with pins GAIN1 (MSB) and GAIN0 (LSB). By using AVDD as the reference input, the bipolar input ranges from ±2.5V to ±19.5mV, while the unipolar ranges from 2.5V to 19.5mV. When the PGA is set to 1 or 2, the absolute inputs can go rail-to-rail without significant performance degradation. However, the inputs of the ADS1232/4 are protected with internal diodes connected to the power-supply rails. These diodes will clamp the applied signal to prevent it from damaging the input circuitry. On the other hand, when the PGA is set to 64 or 128, the operating input range is limited to (AGND + 1.5V) to (AVDD – 1.5V), in order to prevent saturating the differential front-end circuitry and degrading performance.

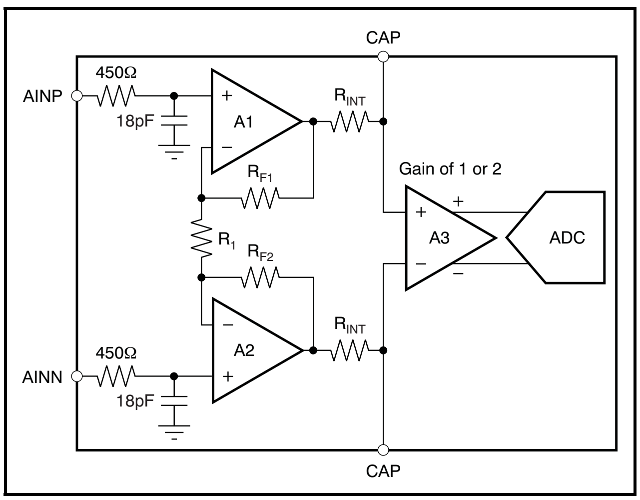


Figure 19. Simplified Diagram of the PGA

Bypass Capacitor

By applying a 0.1µF external capacitor (C_{EXT}) across two capacitor pins and the combination of the internal 2kΩ resistor R_{INT} on-chip, a low-pass filter (with a corner frequency of 720Hz) is created to bandlimit the signal path prior to the modulator input. This low-pass filter serves two purposes. First, the input signal is bandlimited to prevent aliasing as well as to filter out the high-frequency noise. Second, it attenuates the chopping residue from the PGA (for gains of 64 and 128 only) to improve temperature drift performance. It is not required to use high quality capacitors (such as ceramic or tantalum capacitors) for a general application. However, high quality capacitors such as poly are recommended for high linearity applications.

VOLTAGE REFERENCE INPUTS (REFP, REFN)

The voltage reference used by the modulator is generated from the voltage difference between REFP and REFN: V_{REF} = REFP – REFN. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, a switching buffer circuitry is used to reduce the input equivalent capacitance. A simplified diagram of the circuitry on the reference inputs is shown in Figure 20. The switches and capacitors can be modeled with an effective impedance of:

$$Z_{EFF} = \frac{1}{2 f_{MOD} C_{BUF}}$$

Where:

f_{MOD} = modulator sampling frequency (76.8kHz)

C_{BUF} = input capacitance of the buffer

For the ADS1232/4:

$$Z_{EFF} = \frac{1}{(2)(76.8\text{kHz})(32.5\text{fF})} = 200\text{M}\Omega$$

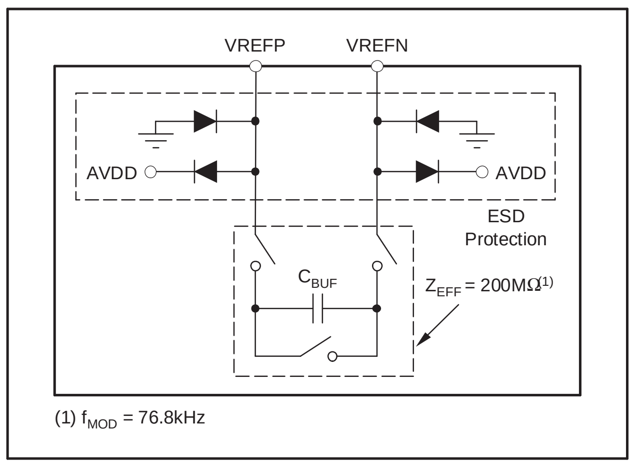


Figure 20. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

GND – 100mV < (REFP or REFN) < AVDD + 100mV

CLOCK SOURCES

The ADS1232/4 can use an external clock source, external crystal, or internal oscillator to accommodate a wide variety of applications. Figure 21 shows the equivalent circuitry of the clock source. The CLK_DETECT block determines whether the crystal oscillator/external clock signal is applied to the CLKIN/XTAL1 pin so that the internal oscillator is bypassed or activated. When the CLKIN/XTAL1 pin frequency is above ~200kHz, the CLK_DETECT output goes low and shuts down the internal oscillator. When the XIN pin frequency is below ~200kHz, the CLK_DETECT output goes high and activates the internal oscillator. It is highly recommended to hard-wire the CLKIN/XTAL1 pin to ground when the internal oscillator is chosen.

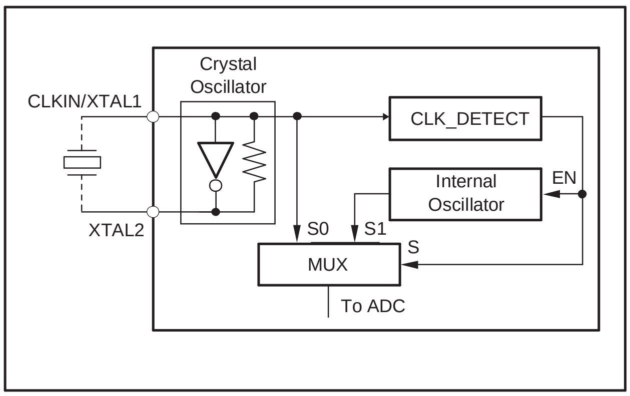


Figure 21. Equivalent Circuitry of the Clock Source

When the clock source is a crystal, simply connect the 4.9152MHz crystal across the CLKIN/XTAL1 and XTAL2 pins. Table 6 shows the recommended part numbers. Due to the low-power design of the parallel resonant driver circuitry onboard, both the CLKIN/XTAL1 and XTAL2 pins are only for use with external crystals; they should not be used as clock output drivers for external circuitry. No external capacitors are used with the crystal; it is recommended to place the crystal close to the part in order to reduce board stray capacitance for both the CLKIN/XTAL1 and XTAL2 pins and to insure proper operation.

Table 6. Recommended Crystals

MANUFACTURER	FREQUENCY	PART NUMBER
ECS	4.9152MHz	ECS-49-20-1
ECS	4.9152MHz	ECS-49-20-4

An external oscillator may be used by driving the CLKIN/XTAL1 pin directly. The Electrical Characteristics table shows the allowable frequency range. The clock input may be driven with 5V logic, regardless of the DVDD or AVDD voltage.

FREQUENCY RESPONSE

The ADS1232/4 use a sinc^4 digital filter with the frequency response (f_{CLK} = 4.9152MHz) shown in Figure 22. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a –3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

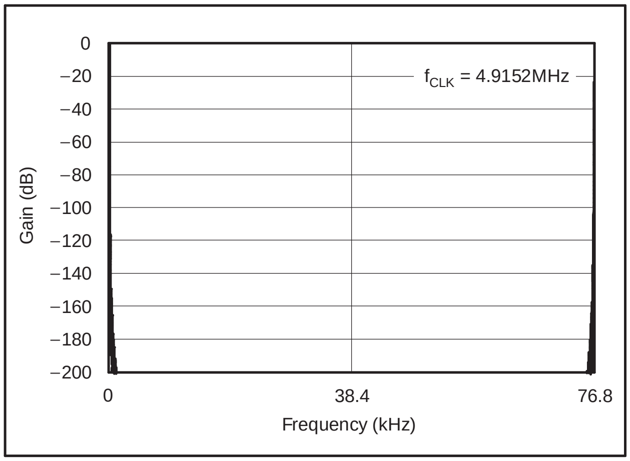


Figure 22. Frequency Response

To help see the response at lower frequencies, Figure 23(a) illustrates the response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc^4 filter is that every frequency notch has four zeros on the same location. This response, combined with the low drift internal oscillator, provides an excellent normal-mode rejection of line-cycle interference.

Figure 23(b) shows the zoom in plot for both 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate). With only a ±3% variation of the internal oscillator, over 100dB of normal-mode rejection is achieved.

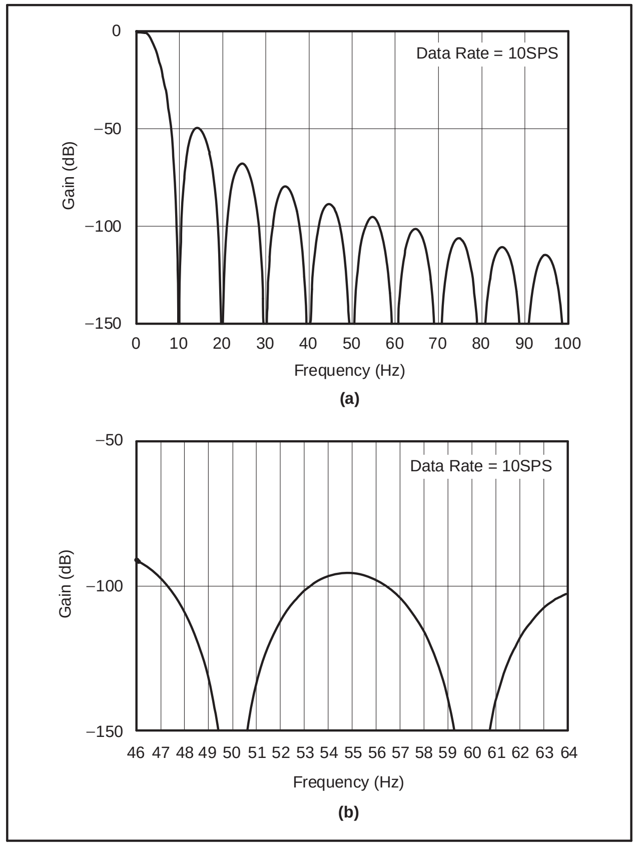


Figure 23. Frequency Response Out To 100Hz

The ADS1232/4 data rate and frequency response scale directly with clock frequency. For example, if f_{CLK} increases from 4.9152MHz to 6.144MHz when the SPEED pin is tied high, the data rate increases from 80SPS to 100SPS, while notches also increase from 80Hz to 100Hz. Note that this is only possible when the external clock source is applied.

SETTLING TIME

After changing the input multiplexer, or selecting the onboard temperature sensor (ADS1232 only), the first data is fully settled. In both the ADS1232/4, the digital filter is allowed to settle after toggling any of the A1, A0, or TEMP pins. Toggling any of these digital pins will hold the DRDY/DOUT line high until the digital filter is fully settled. For example, if A0 changes from low to high, selecting a different input channel, DRDY/DOUT immediately goes high, and DRDY/DOUT goes low when fully-settled data is ready for retrieval. There is no need to discard any data. Figure 24 shows the timing of the DRDY/DOUT line as the input multiplexer changes.

In certain instances, large changes in input will require settling time. For example, an external multiplexer in front of the ADS1232/4 can put large changes in input voltage by simply switching input channels. Abrupt changes in the input will require four data cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input will be required to get fully-settled data. Discard the first four readings because they will contain only partially-settled data. Figure 25 illustrates the settling time for the ADS1232/4 in Continuous Conversion Mode.

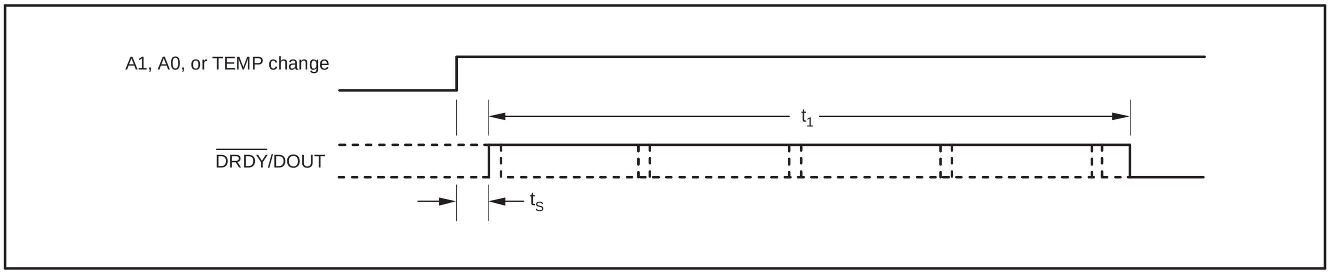


Figure 24. Example of Settling Time After Changing the Input Multiplexer

SYMBOL	DESCRIPTION(1)		MIN	MAX	UNITS
t_S	Setup time for changing any of the A1, A0, or TEMP pins		40	50	µs
t_1	Settling time (DRDY/DOUT held high)	SPEED = 1	51	51	ms
		SPEED = 0	401	401	ms

(1) Values given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

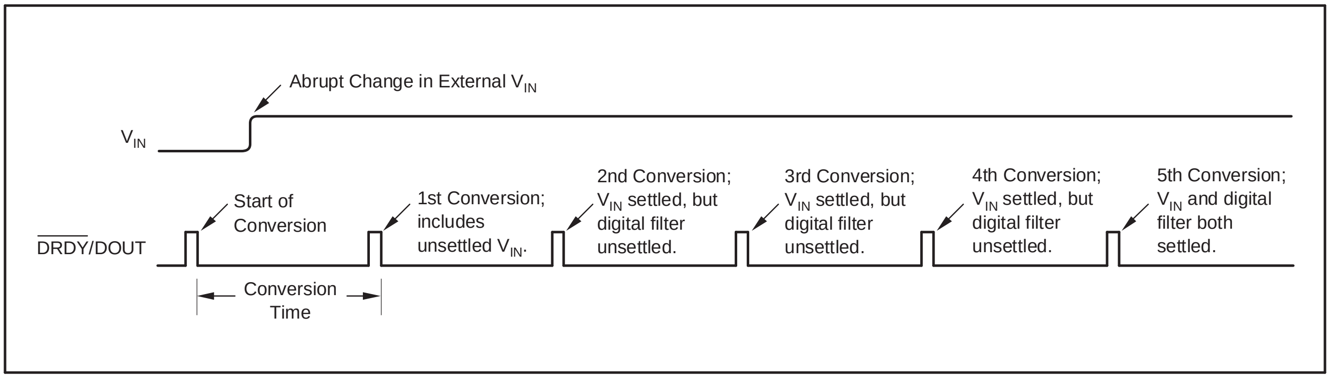


Figure 25. Settling Time in Continuous Conversion Mode

DATA RATE

The ADS1232/4 data rate is set by the SPEED pin, as shown in Table 7. When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

Table 7. Data Rate Settings

SPEED PIN	DATA RATE	
	Internal Oscillator or 4.9152MHz Crystal	External Oscillator
0	10SPS	f_{CLKIN} / 491,520
1	80SPS	f_{CLKIN} / 61,440

DATA FORMAT

The ADS1232/4 output 24 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of $0.5V_{REF}/(2^{23} - 1)$. The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 8 summarizes the ideal output codes for different input signals.

Table 8. Ideal Output Code vs Input Signal(1)

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE
$\geq +0.5V_{REF}$/Gain	7FFFFFh
$(+0.5V_{REF}/\text{Gain})/(2^{23} - 1)$	000001h
0	000000h
$(-0.5V_{REF}/\text{Gain})/(2^{23} - 1)$	FFFFFFh
$\leq -0.5V_{REF}$/Gain	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

DATA READY/DATA OUTPUT ($\overline{\text{DRDY}}$/DOUT)

This digital output pin serves two purposes. First, it indicates when new data is ready by going low. Afterwards, on the first rising edge of SCLK, the $\overline{\text{DRDY}}$/DOUT pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data is shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. It will then stay high until new data is ready. This configuration is useful when polling on the status of $\overline{\text{DRDY}}$/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. As with CLK, this input may be driven with 5V logic regardless of the DVDD or AVDD voltage. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise-and-fall times of SCLK are less than 50ns.

DATA RETRIEVAL

The ADS1232/4 continuously convert the analog input signal. To retrieve data, wait until DRDY/DOUT goes low, as shown in Figure 26. After this occurs, begin shifting out the data by applying SCLKs. Data is shifted out MSB first. It is not required to shift out all 24 bits of data, but the data must be retrieved before new data is updated (within t_7) or else it will be overwritten. Avoid data retrieval during the update period (t_6). DRDY/DOUT remains at the state of the last bit shifted out until it is taken high (see t_6), indicating that new data is being updated. To avoid having DRDY/DOUT remain in the state of the last bit, the user can shift SCLK to force DRDY/DOUT high, as shown in Figure 27. This technique is useful when a host controlling the device is polling DRDY/DOUT to determine when data is ready.

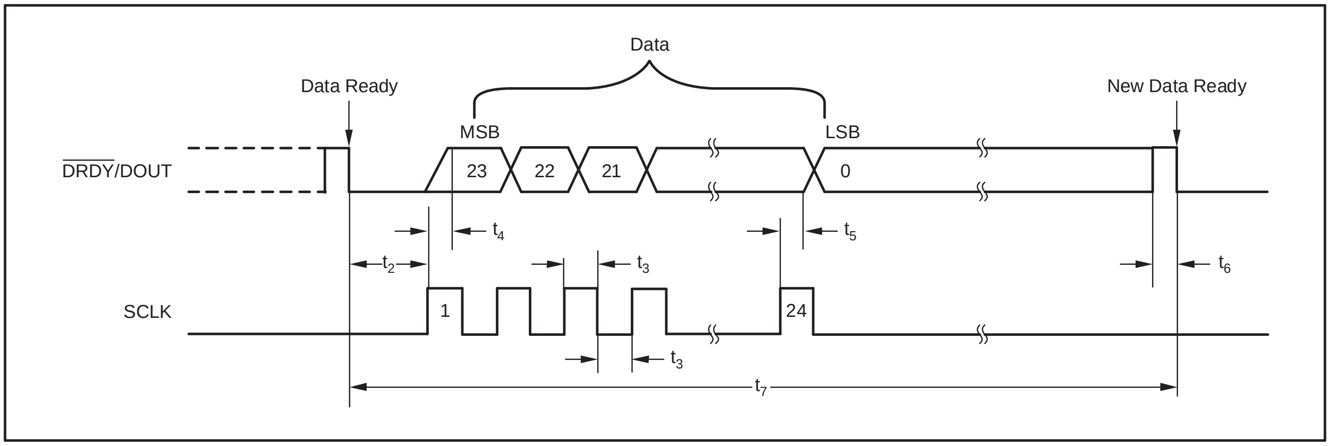


Figure 26. Data Retrieval Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t_2	DRDY/DOUT low to first SCLK rising edge		0			ns
t_3	SCLK positive or negative pulse width		100			ns
t_4	SCLK rising edge to new data bit valid: propagation delay				50	ns
t_5	SCLK rising edge to old data bit valid: hold time		0			ns
t_6 (1)	Data updating: no readback allowed		39			µs
t_7 (1)	Conversion time (1/data rate)	SPEED = 1		12.5		ms
		SPEED = 0		100		ms

(1) Values given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

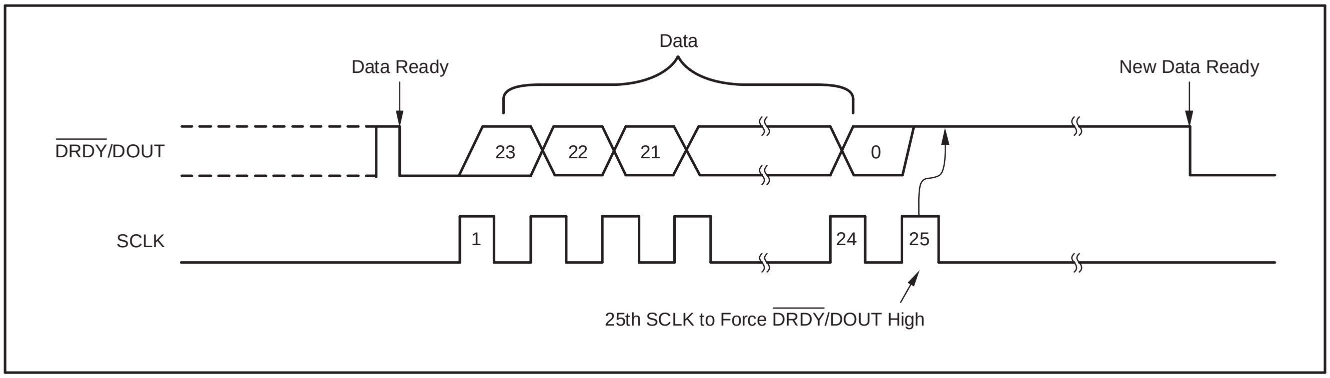


Figure 27. Data Retrieval with DRDY/DOUT Forced High Afterwards

OFFSET CALIBRATION

Offset calibration can be initiated at any time to remove the ADS1232/4 inherited offset error. To initiate offset calibration, apply at least two additional SCLKs after retrieving 24 bits of data. Figure 28 shows the timing pattern. The 25th SCLK will send DRDY/DOUT high. The falling edge of the 26th SCLK will begin the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK; however, activity on SCLK should be minimized during offset calibration for best results.

When the calibration is completed, DRDY/DOUT goes low, indicating that new data is ready. The analog input pins are disconnected within the ADC and the appropriate signal is applied internally to perform the calibration. The first conversion after a calibration is fully settled and valid for use. The offset calibration takes exactly the same time as specified in (t_8) right after the falling edge of the 26th SCLK.

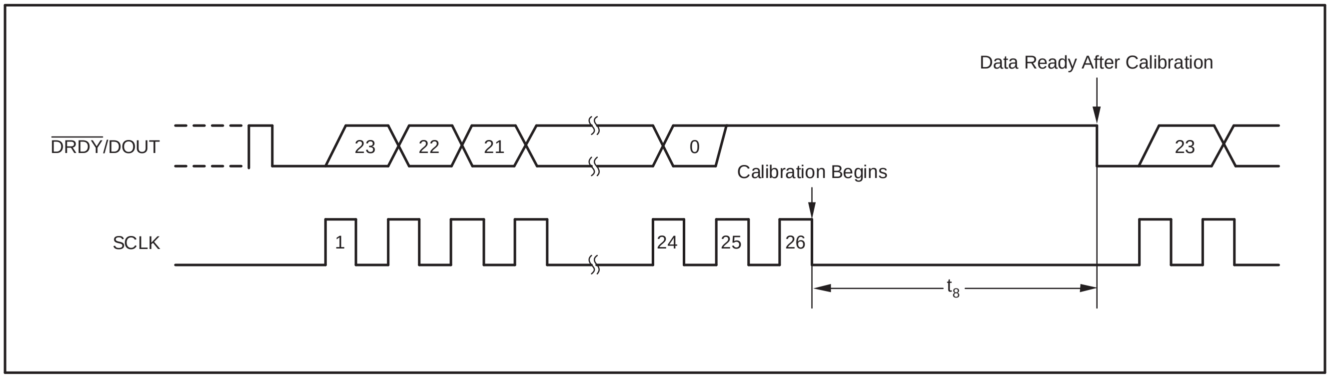


Figure 28. Offset-Calibration Timing

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t_8 (1)	First data ready after calibration	SPEED = 1	101.28	101.29	ms
		SPEED = 0	801.02	801.03	ms

(1) Values given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

STANDBY MODE

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. In Standby mode, the entire analog circuitry is powered down and only the clock source circuitry is awake to reduce the wake-up time from the Standby mode. To enter Standby mode, simply hold SCLK high after $\overline{DRDY}$/DOUT goes low; see Figure 29. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand.

When t_{10} has passed with SCLK held high, Standby mode will activate. $\overline{DRDY}$/DOUT stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode is valid.

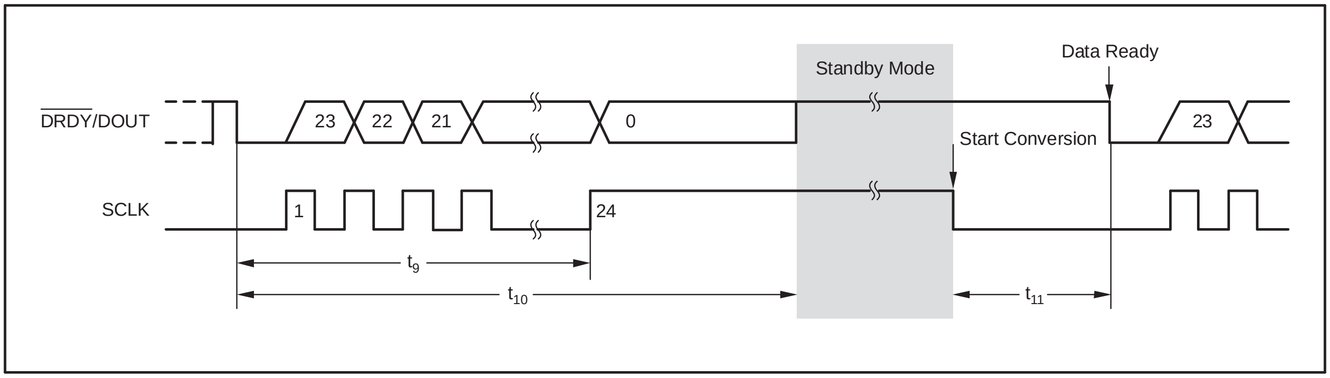


Figure 29. Standby Mode Timing (can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t_9 (1)	SCLK high after $\overline{DRDY}$/DOUT goes low to activate Standby mode	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	ms
t_{10} (1)	Standby mode activation time	SPEED = 1	12.46		ms
		SPEED = 0	99.96		ms
t_{11} (1)	Data ready after exiting Standby mode	SPEED = 1	52.51	52.51	ms
		SPEED = 0	401.8	401.8	ms

(1) Values given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

STANDBY MODE WITH OFFSET-CALIBRATION

Offset-calibration can be set to run immediately after exiting Standby mode. This is useful when the ADS1232/4 is put in Standby mode for long periods of time, and offset-calibration is desired afterwards to compensate for temperature or supply voltage changes.

To force an offset-calibration with Standby mode, shift 25 SCLKs and take the SCLK pin high to enter Standby mode. Offset-calibration then begins after wake-up; see Figure 30 for the appropriate timing. Note the extra time needed after wake-up for calibration before data is ready. The first data after Standby mode with offset-calibration is fully settled and can be used right away.

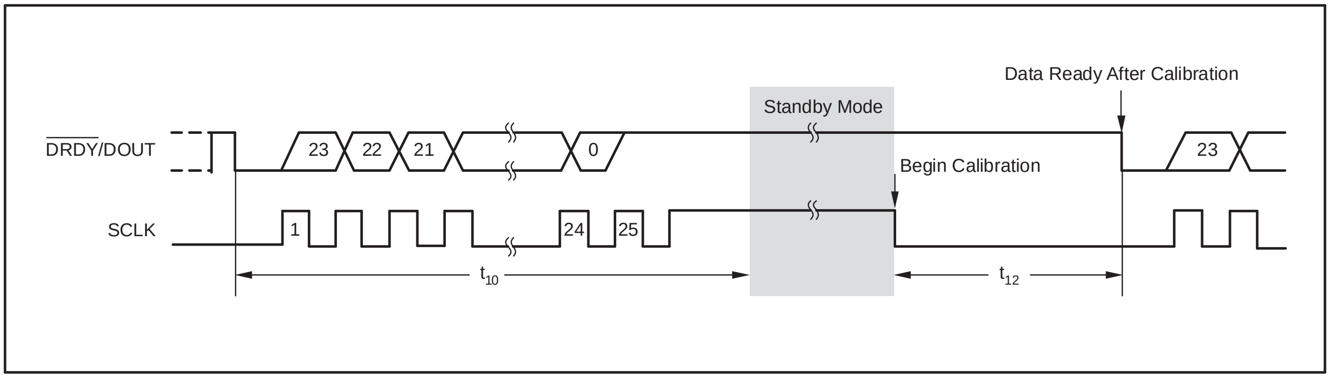


Figure 30. Standby Mode with Offset-Calibration Timing (can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t_{12} (1)	Data ready after exiting Standby mode and calibration	SPEED = 1	103	103	ms
		SPEED = 0	803	803	ms

(1) Values given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the $\overline{\text{PDWN}}$ pin low. Power-Down mode also resets the entire circuitry to free the ADC circuitry from locking up to an unknown state. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand. Figure 31 shows the wake-up timing from Power-Down mode.

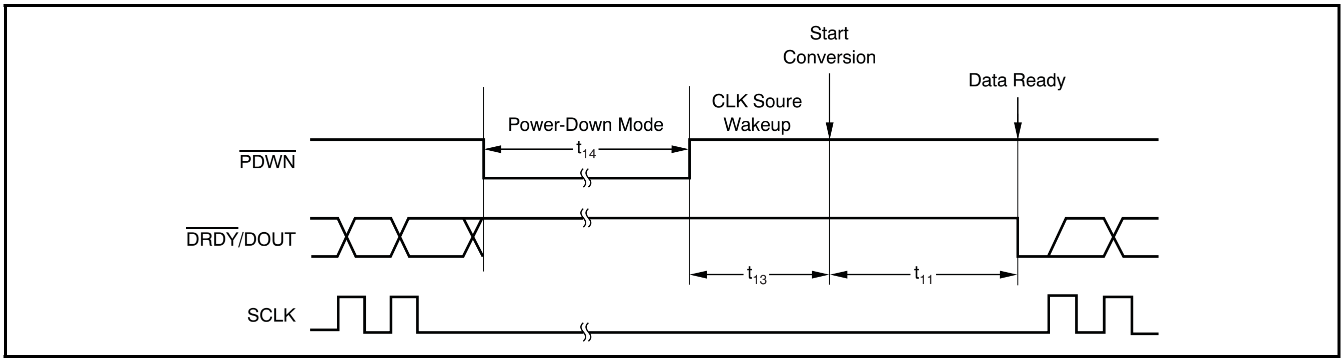


Figure 31. Wake-Up Timing from Power-Down Mode

SYMBOL	DESCRIPTION		TYP	UNITS
t_{13}	Wake-up time after Power-Down mode	Internal clock	7.95	µs
		External clock	0.16	µs
		Crystal oscillator(1)	5.6	ms
t_{14}(2)	PDWN pulse width		26 (min)	µs

(1) No capacitors on CLKIN/XTAL1 or XTAL2 outputs.
(2) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, the scale is proportional to the CLK period except for a ±3% variation when an internal oscillator is used.

APPLICATION EXAMPLES

Weigh-Scale System

Figure 32 shows a typical ADS1232 hook-up as part of a weigh-scale system. In this setup, the ADS1232 is configured to channel one input with a gain of 128 at a 10SPS data rate. Note that the internal oscillator is used by grounding the CLKIN/XTAL1 pin. The user can also apply either a 4.9152MHz crystal across the CLKIN/XTAL1 and XTAL2 pins, or simply apply a clock to the CLKIN/XTAL1 pin. For a typical 2mV/V load cell, the maximum output signal is approximately 10mV for a single +5V excitation voltage. The ADS1232/4 can achieve 18.4 noise-free bits at 10SPS when the PGA = 128 (refer to Table 1). With the extra software filtering/averaging (typically done by a microprocessor), an extra bit can be expected.

$$\text{Noise-Free Counts} = \left(2^{BIT_{Eff}}\right)\left(\frac{FS_{LC}}{FS_{AD}}\right)$$

Where:

BIT_{EFF} = effective noise-free bits (18.4 + 1 bit from software filtering/averaging)

FS_{LC} = full-scale output of the load cell (10mV)

FS_{AD} = full-scale input of the ADS1232/4 (39mV when PGA = 128)

Therefore:

$$\text{Noise-Free Counts} = \left(2^{(18.4+1)}\right)\left(\frac{10\text{mV}}{39\text{mV}}\right) = 177,385$$

With +5V supply voltage, 177,385 noise-free counts can be expected from the ADS1232/4 with the onboard PGA set to 128.

Thermocouple

See Figure 33 for the ADS1232 in a thermocouple application. In this example, a type *k* thermocouple is used; the temperature range is from –260°C to +900°C when the gain is set to 64 to maximize the full input range of the ADS1232. R_1 and a REF1004-2.5V are used to set the common-mode voltage to 2.5V for ungrounded junction thermocouples. With a gain of 128, the ADS1232 input has a typical noise of $17nV_{RMS}$ for extremely high-resolution applications.

If either a wider temperature range application is required (up to +1350°C, for example), or a grounded junction thermocouple is used, pin 1 of the thermocouple can be grounded (see Figure 34). When the gain is set to 2, the ADS1232 input has a typical 500nV offset error and a noise level of $270nV_{RMS}$, which is good for all kinds of low-voltage output sensors. Note that to calculate the actual thermocouple temperature, the ADS1232 internal temperature sensor can be accessed in order to measure the cold junction temperature along with the thermocouple reading.

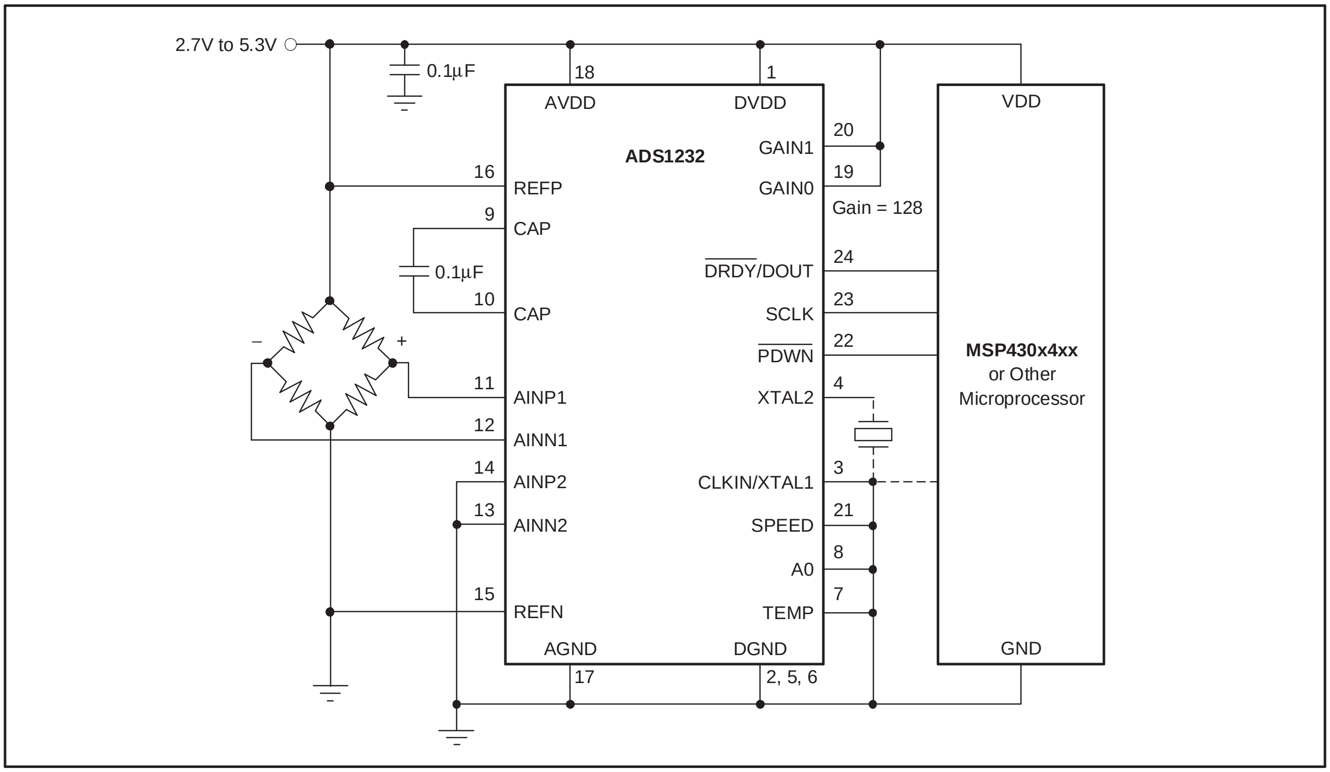


Figure 32. Weigh Scale Application

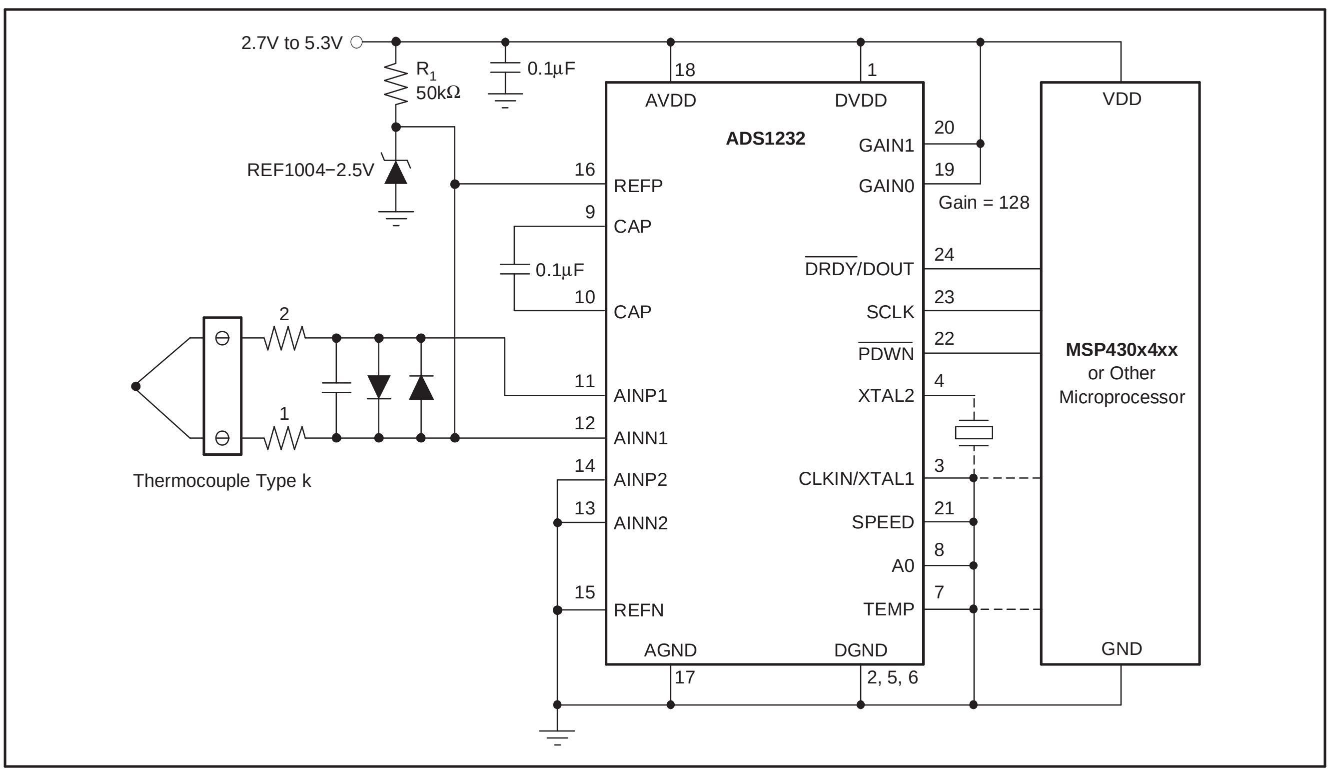


Figure 33. Ungrounded Junction Thermocouple Application

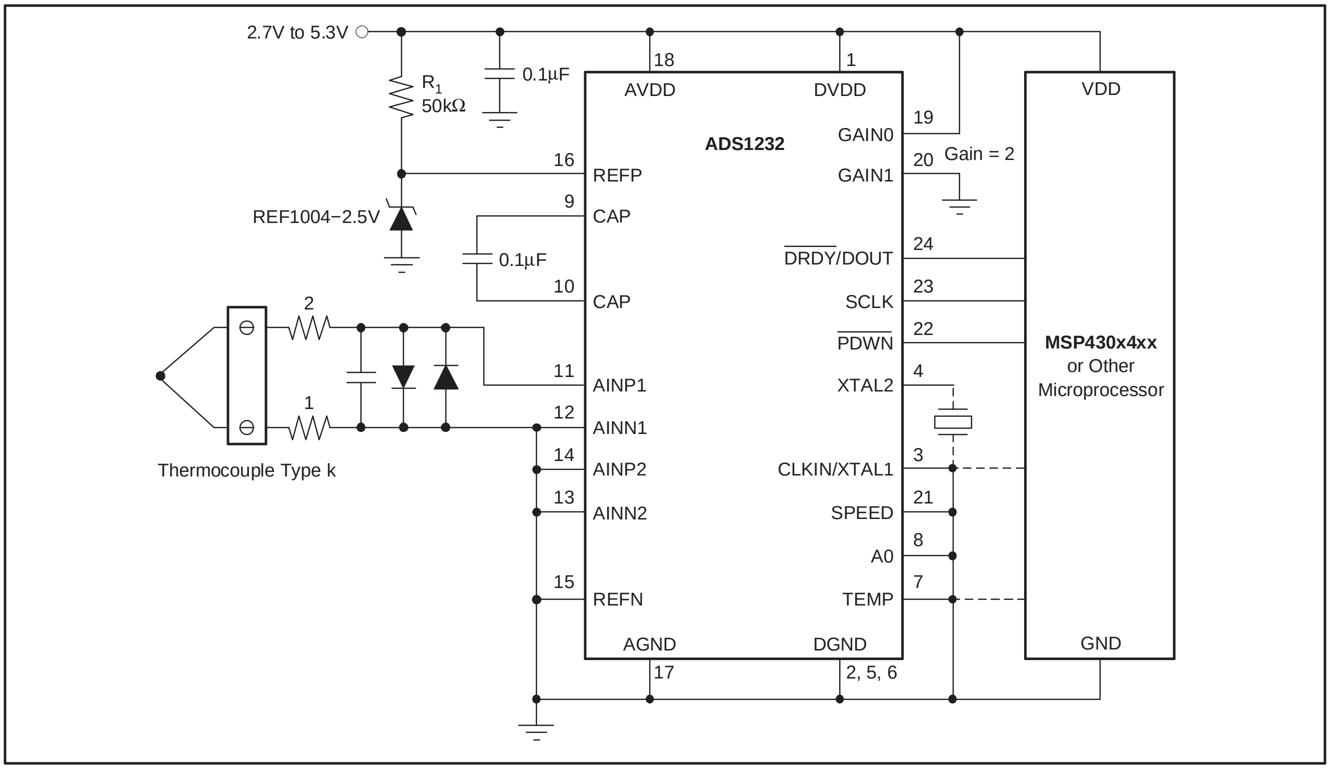


Figure 34. Grounded Junction Thermocouple Application

RTDs and Thermistors

Figure 35 shows a typical schematic for a style 2 (three-wire) RTD application. R_1 and R_2 are used to excite the RTD as well as establish the common-mode voltage of the ADS1232 PGA. By using both differential channels of the ADS1232, the temperature change in lead resistance, R_L, can be eliminated. This condition is accomplished by using the following formula:

(AINP1 – AINN1) – 2(AINP2 – AINN2).

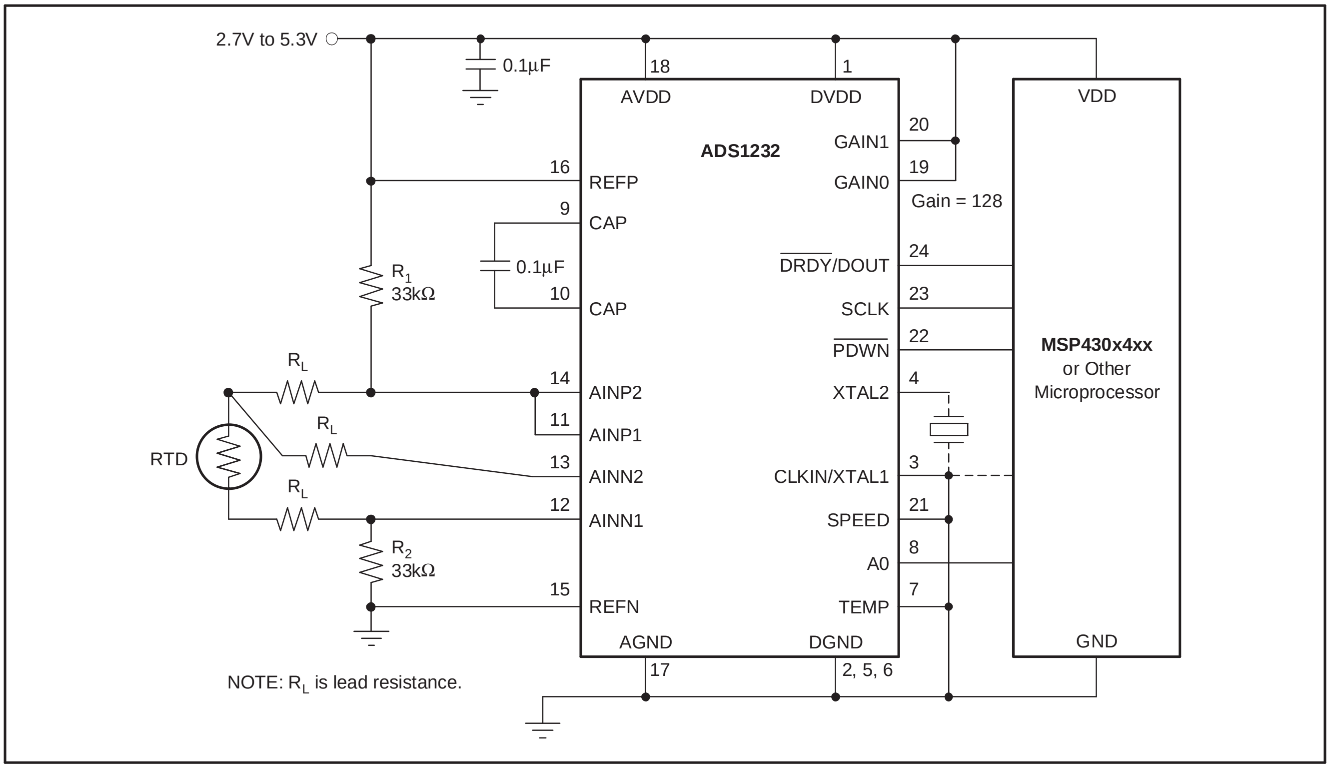


Figure 35. Style 2 (Three-Wire) RTD Schematic

SUMMARY OF SERIAL INTERFACE WAVEFORMS

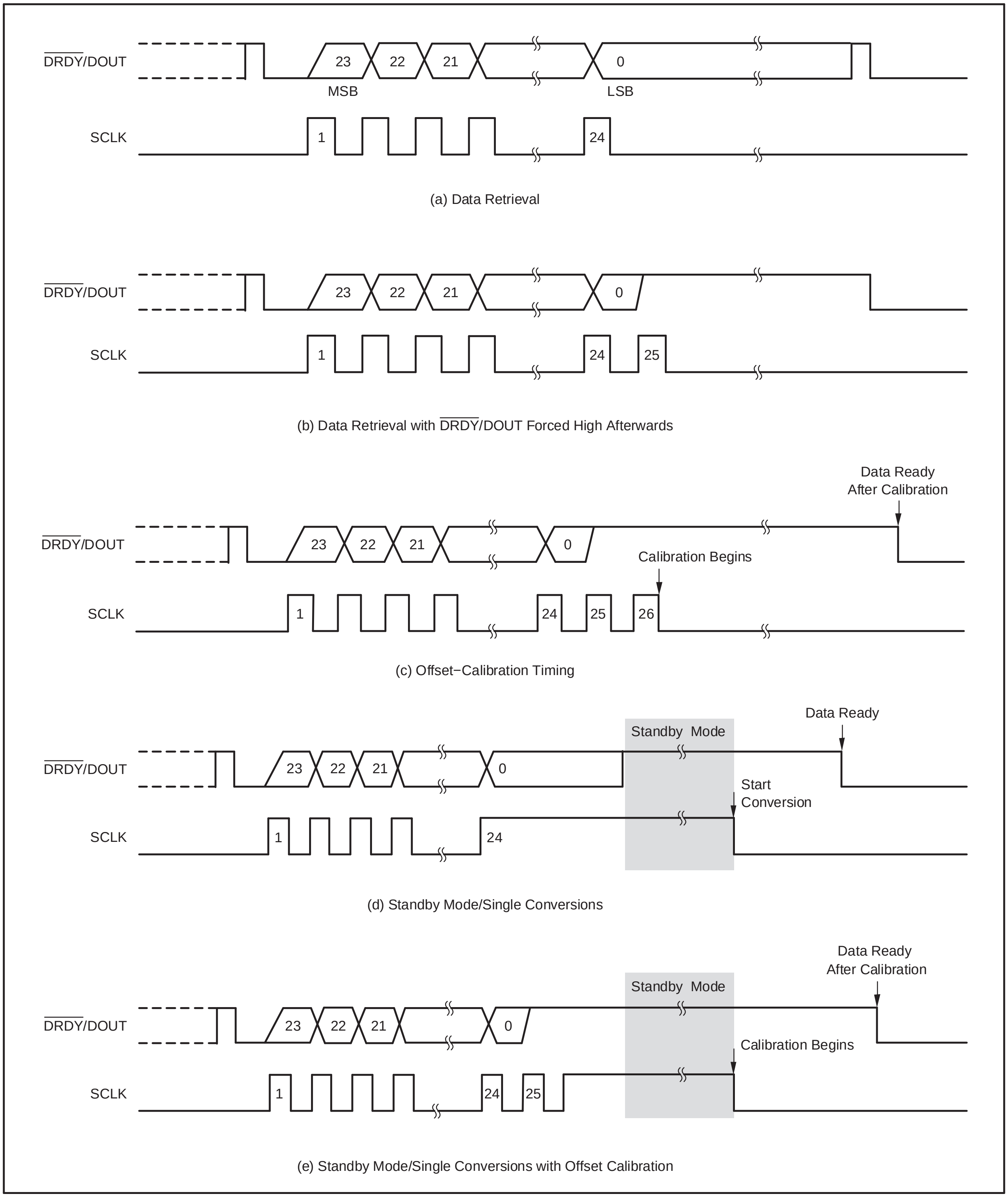


Figure 36. Summary of Serial Interface Waveforms

Changes from B Revision (September 2005) to C Revision	Page
• Deleted last row from Absolute Maximum Ratings table.	2
• Changed *Analog Inputs* section of Electrical Characteristics table.	3
• Changed the typical value in last row of *Voltage Reference Input* section of Electrical Characteristics table.	3
• Added footnote 1 to Table 1, Table 2, Table 3, and Table 4.	5
• Changed fourth sentence in Temperature Sensor section of Overview.	11
• Added fifth and sixth sentences to Temperature Sensor section of Overview.	11
• Added fourth and fifth sentences to Low-Noise PGA section of Overview.	12
• Changed Figure 19.	12
• Changed t_{11} to t_{10} in third paragraph of Standby Mode section of Overview.	19
• Changed min and max variables of t_{10} row in table below Figure 29.	19
• Changed Figure 31.	21
• Added last row and second footnote to table below Figure 31.	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1232IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1232IPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1232IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1232IPWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1234IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1234IPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1234IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1234IPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

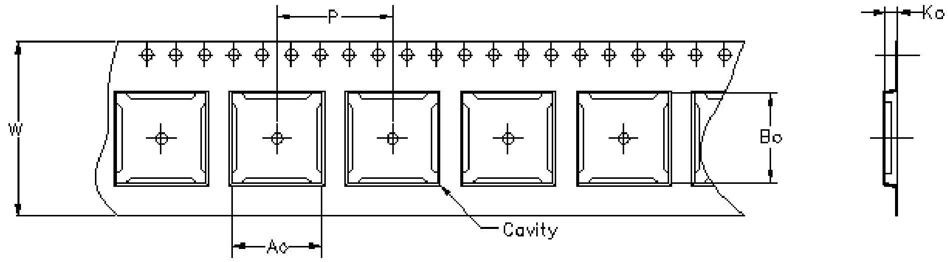
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

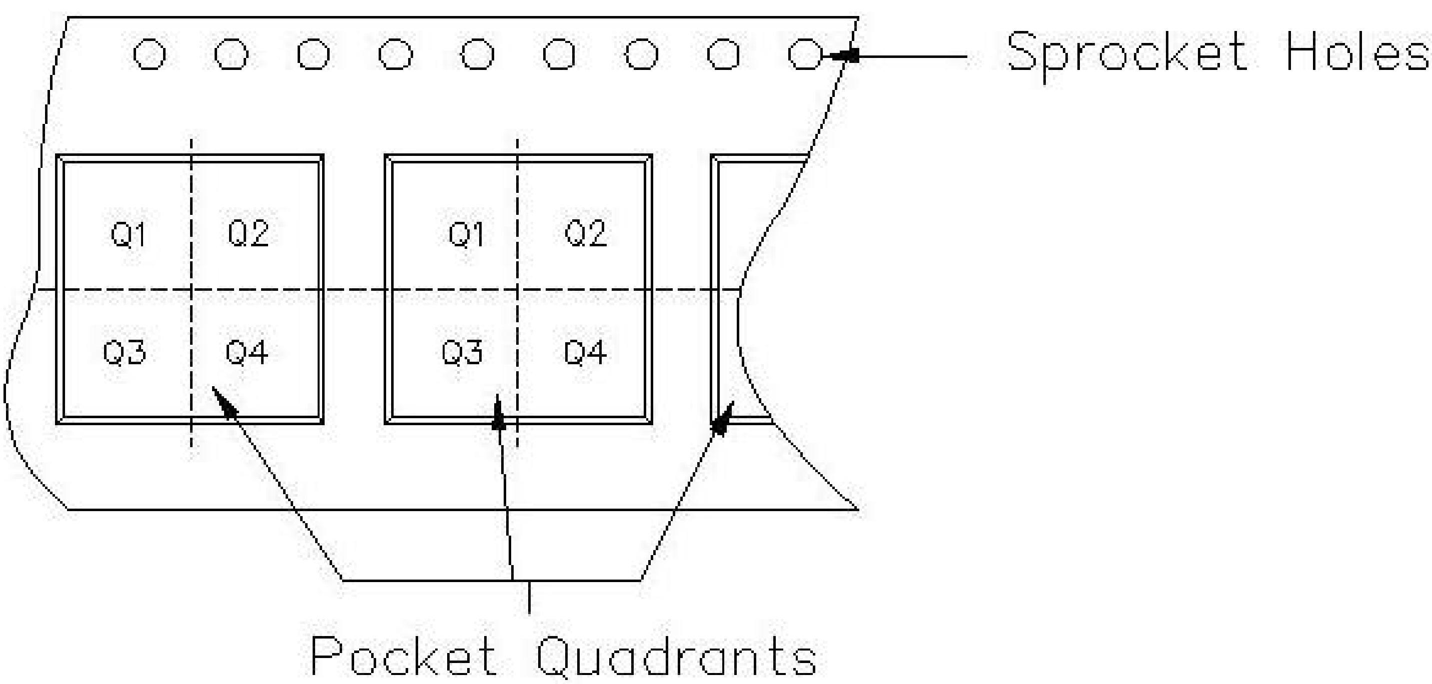
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



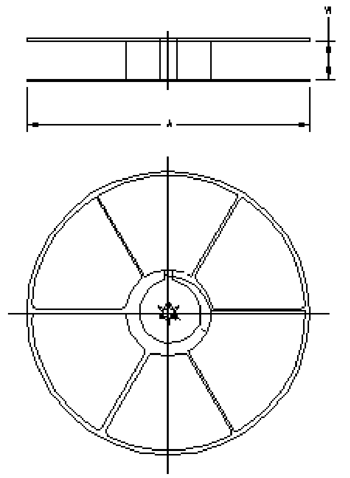
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.



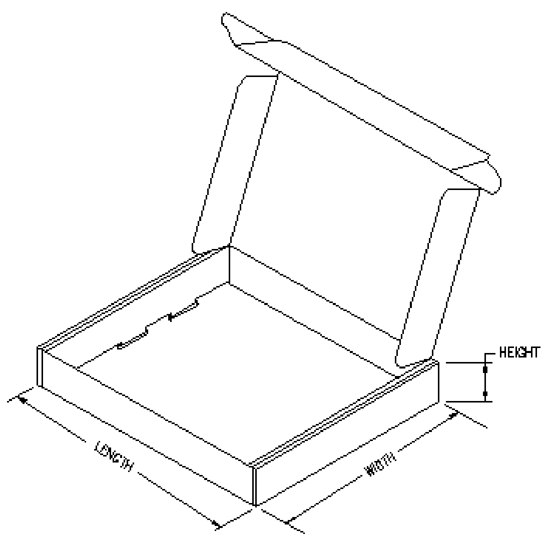
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1234IPWR	PW	28	TAI	330	16	6.9	10.2	1.8	12	16	PKGORNT1TR-MSP



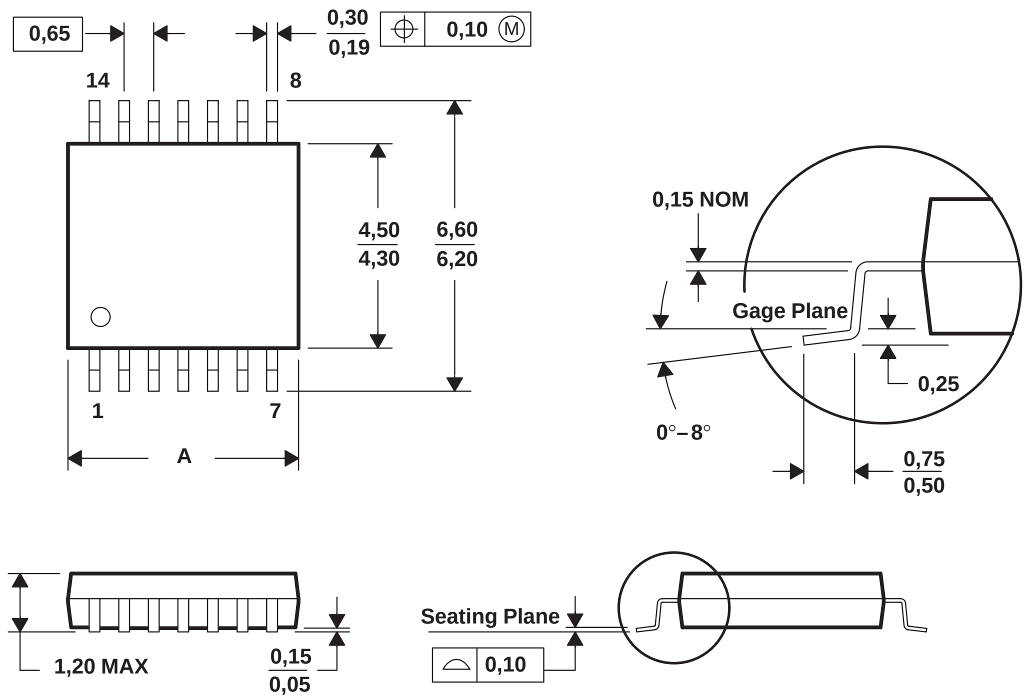
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
ADS1234IPWR	PW	28	TAI	346.0	346.0	33.0



PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153