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FEATURES

- ◆ Blue on Grey STN Type
- ◆ Transflective Mode

MECHANICAL DATA

Item	Value	Unit
Module Dimensions	159.4*101*9.5	mm
Viewing Area	126*71	mm
Resolution	240*128	dots
Dot Size	0.47*0.47	mm
Dot Pitch	0.5*0.5	mm
Weight	160	g

OPTICAL DATA

Item	Symbol	Condition	Min	Typ	Max	Unit
Contrast Ratio	K	Ø=10°, θ=0°, Note 1	-	3.0	-	-
Brightness	-	-	-	10	-	cd/m ²
Viewing Direction	-	-	6			o'clock
Viewing Angle	Ø2 - Ø1	K=1.4, Note 1	-	40	-	degree
Response Time (Rise)	t _R	Ø=10°, θ=0°, Note 1	-	250	400	ms
Response Time (Fall)	t _F	Ø=10°, θ=0°, Note 1	-	300	450	ms

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit
Supply Voltage (Logic)	V _{DD} - V _{SS}	-	0	7	V
Supply Voltage (LC Drive)	V _{DD} - V _{EE}	-	0	22	V
Input Voltage	V _I	-	V _{SS}	V _{DD}	V
Operating Temperature	T _{OP}	Note 4,5	0	50	°C
Storage Temperature	T _{ST}	Note 4,5	-20	60	°C

DATA INTERFACE PIN ASSIGNMENT

Pin No	Symbol	Level	Function
A1	VSS (0V)	-	Ground
A2	VDD (+5V)	-	Power supply for logic
A3	V0	-	Power supply for LCD drive
A4	RS	-	Register select
A5	R/W	-	Read / Write
A6	E	-	Enable
A7-A14	DB0 - DB7	-	Data bus
A15	Not CS	-	Chip select
A16	Not RES	-	Reset
A17	VEE (15.0V)	-	Power supply for LCD drive
A18-A20	NC	-	No connection
E1-E2	VEL	-	Power supply for EL driving

- ◆ Low Power EL Backlight
- ◆ Built-in LCD Controller HD61830B

ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (Logic)	V _{DD} - V _{SS}	-	4.75	5.0	5.25	V
Supply Voltage (LC Drive)	V _{EE} - V _{SS}	-	-14.5	-15.0	-15.5	V
Supply Current	I _{DD}	Note 2	-	6.0	-	mA
	I _{EE}	Note 2	-	4.0	-	mA
Input Voltage (High Level)	V _{IH}	High Level	0.8* VDD	-	VDD	V
Input Voltage (Low Level)	V _{IL}	Low Level	0	-	0.2* VDD	V
Frame Frequency	f _{FLM}	-	-	75	-	Hz
Duty Ratio		-		1/128	-	-
Recommended LC Drive Voltage	V _{DD} - V _O	Duty=1/128 T=0°C, Ø=10°, Note 3	-	16.9	-	V
		Duty=1/128 T=25°C, Ø=10°, Note 3	-	15.8	-	V
		Duty=1/128 T=40°C, Ø=10°, Note 3	-	15.4	-	V
Backlight Tile Voltage	V _{EL}	f _{EL} =400Hz	-	100	-	Vrms
Backlight Lamp Frequency	f _{EL}	-	-	400	-	Hz
Backlight Tile Current	I _{EL}	V _{EL} =100Vrms, f _{EL} =400Hz	-	-	160	mA Arms

TIMING CHARACTERISTICS

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	tCYC	1000	-	-	ns
Enable pulse width (High level)	tWEH	450	-	-	ns
Enable pulse width (Low level)	tWEL	450	-	-	ns
Enable rise time	tEr	-	-	25	ns
Enable fall time	tEf	-	-	25	ns
Set up time of CS, R/W, RS	tAS	140	-	-	ns
Set up time of Input Data	tDIS	225	-	-	ns
Data delay time	tDD	-	-	225	ns
Hold time of Data	tH	10	-	-	ns
Hold time of CS, R/W, RS	tAH	10	-	-	ns
Data hold time	tDH	20	-	-	ns

CONNECTORS

Connector	
No special connector required	

- Note1:Definition of optical data, see page XXX
- Note2:fFLM=75Hz, VDD-V0=15.8V, D=GND(VSS)
- Note3:Recommended LC driving voltage may fluctuate about +- 0.5V by each module
- Note4:Background colour of the LCD changes depending on temperature. Between 40-50°C optical characteristics of the LCD like contrast and viewing angle change but the LCD remains readable.
- Note5:Storage at -20°C < 48 hr.

MECHANICAL DIMENSIONS

159.4
152.4 $\pm$ 0.3
142.4
126.0 $\pm$ 0.3
0.50*239+0.47=119.97 $\pm$ 0.1
3.5
8.5
3.5
0.5
8.1
(3.5)
(3.0)
0.50*127+0.47=63.97 $\pm$ 0.1
71.0 $\pm$ 0.3
87.2
94.0 $\pm$ 0.3
101.0
E1
E2
EL SEALING AREA
1.5 MAX
1.5 MAX
9.5 MAX.
4.9
1.2 $\pm$ 0.2
A1
A20
B1
B10
4-AB 0
+/-0.5
12.0
2.54
48.26 $\pm$ 0.3
2.5
(3.5)
2.54
(3.5)
22.86 $\pm$ 0.3
12.0 $\pm$ 0.5
(6.3)

The block diagram illustrates the internal architecture of the LCD module. On the left, the microcontroller (MCU) provides control signals: $\overline{CS}$, $\overline{RES}$, RS , R/W , E , and data bus $DB0$ to $DB7$. An 8-bit data bus connects the MCU to the **CONTROLLER HU31820**. The controller is also connected to an **OSC** (oscillator) and **RAM** (13 words, 8 bits each). The controller outputs **FLM** (Frame Lock Manager) and **CL1**, **CL2** (Column Locks) signals to the **IC1** and **IC2** (Column Drivers). **IC1** and **IC2** are 64-bit drivers that output **X1** to **X128** and **Y1** to **Y240** signals to the **LCD 240*128**. The LCD is connected to the **IC3**, **IC4**, and **IC5** (Row Drivers) via 80-bit data buses. The **IC3**, **IC4**, and **IC5** are 80-bit drivers that output **80** signals to the LCD. The **IC3**, **IC4**, and **IC5** are also connected to the **VLCD** (Vertical Lock) and **M'** (Master) signals. The **POWER CIRCUIT** provides **VDD**, **VSS**, **VO**, and **VEE** signals to the module. The **TIMING** block provides **M'** and **VLCD** signals to the **IC3**, **IC4**, and **IC5**.

VR: 10~20K Ω

The diagram shows the timing relationships for the LCM (LCM to MPU) interface. The signals and their timing parameters are as follows:

- E**: Enable signal. Timing parameters: t_{Er} (rise time), t_{Ef} (fall time).
- CS, R/W, RS**: Chip select, read/write, and reset signals. Timing parameters: t_{AS} (access time), t_{AH} (hold time).
- DB0-7 (MPU TO LCM)**: Data bus from MPU to LCM. Timing parameters: t_{DIS} (discharge time), t_H (hold time).
- DB0-7 (LCM TO MPU)**: Data bus from LCM to MPU. Timing parameters: t_{DD} (data delay), t_{DH} (data hold time).

The diagram also indicates the timing for the LCM (LCM to MPU) interface, showing the relationship between the LCM and the MPU. The timing parameters for the LCM (LCM to MPU) are:

- t_{WEH} : Write enable high pulse width.
- t_{WEL} : Write enable low pulse width.
- t_{Er} : Enable rise time.
- t_{Ef} : Enable fall time.
- t_{AS} : Address setup time.
- t_{AH} : Address hold time.
- t_{DIS} : Data input discharge time.
- t_H : Data input hold time.
- t_{DD} : Data output delay time.
- t_{DH} : Data output hold time.

The figure contains two timing diagrams. The left diagram, labeled 'POWER ON', shows VDD rising to 4.75V, followed by a delay of 0-50 ms before the SIGNAL rises. After the SIGNAL rises, there is a delay of 0 ms min. before VEE falls. The right diagram, labeled 'POWER OFF', shows VDD falling from 4.75V, followed by a delay of 0-50 ms before the SIGNAL falls. After the SIGNAL falls, there is a delay of 0 ms min. before VEE rises. The label 'VALID DATA' is placed between the two diagrams, indicating the period when the signal is valid.