Intel 8051 Family – Standard PODs

All 8051 family PODs are 8-bit PODs that can be used on iC181, iC1000 and the PowerEmulator unit with the exception of a few PODs, that can not be used on the iC181 unit. Please check the description of the POD if you want to use it with the iC181 Emulator.

Bank switching is supported on non-single chip PODs.

See "In-Circuit Emulation PODs" on page 324 for general POD information.

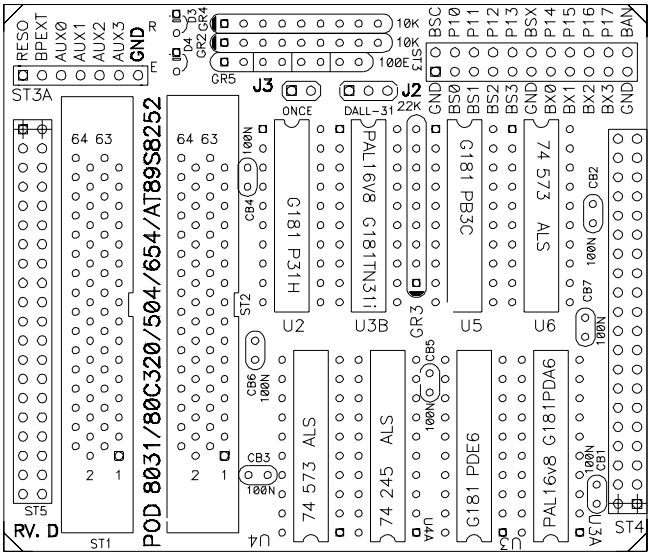
Before connecting the PODs, make sure you have read the technical notes on "Intel 8051 Family" on page 145.

PODs that are described in this part of the manual are, in order of appearance:

Intel 8051 POD Motherboard rev A

Dimensions (mm)	85x72

This motherboard POD is used as a top board for some 8051 Family PODs.



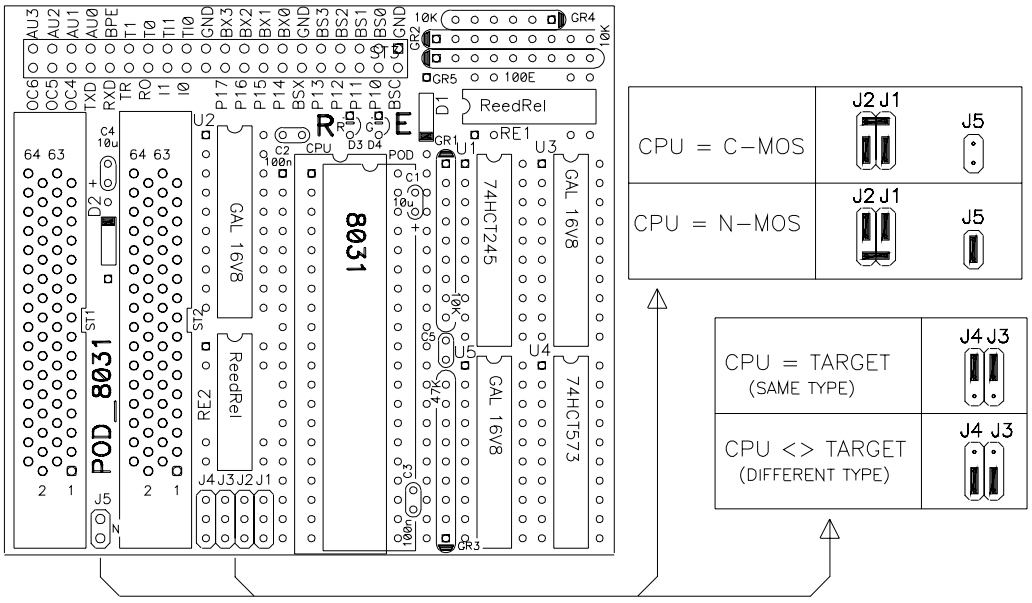
Top board

Intel 8031 POD rev. E, F, G

Ordering code	IC81020		
POD Speed (MHz)	16	24	42
Emulator Speed (ns)	150	90	65
Bank switch support	YES		
Exchange CPU	YES		
Dimensions (mm)	80x74		
Pin 1 position (mm)	41x52		

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



When exchanging CPU's adjust jumpers J1-J5 according to CMOS/NMOS type of the CPU.

Target POD pinout is a standard DIP40.

Emulated CPU
8031, 80C31 - 8032, 80C32
8051, 80C51 (*) - 8052, 80C52 (*)
83C44
80C154 (*)
80C652 - 80C654
80C851
80C410
SAB-C501, SAB-C502

Note: CPUs with internal ROM (*) can only be used if P0 and P1 CPU ports are available for external mode addressing. In such case program that resides in internal ROM must be downloaded.

Signal	Description
INT0-TINT0 INT1-TINT1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.
P1.0 - P1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32k; Bridged=64k
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32k; Bridged=64k
TXD, RXD	Transmit and receive lines for serial channel 0.

ST3 Connector signal description

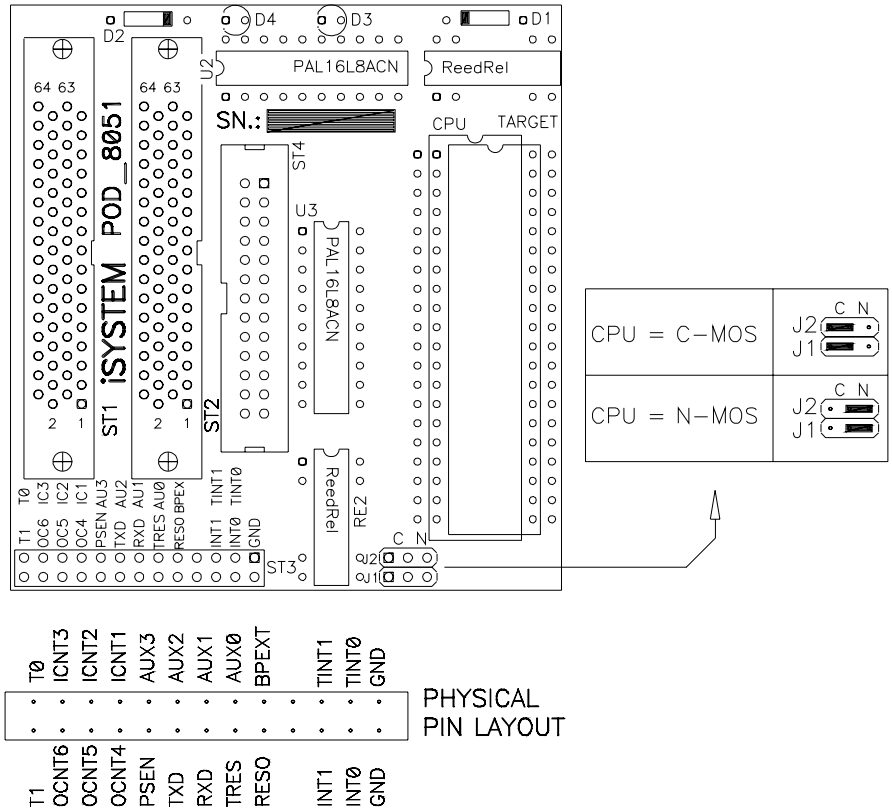
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Intel 8051 POD rev. A

Ordering code	IC81021	
POD Speed (MHz)	12	22
Emulator Speed (ns)	150	90
Bank switch support	NO	
Exchange CPU	NO	
Dimensions (mm)	74x79	
Pin 1 position (mm)	58x59	

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Target POD pinout is a standard DIP40.

Emulated CPU
80C51, 87C51, 89C51
80C52, 87C52, 89C52
83C154
AT89C1051 (*)
AT89C2051 (*)

Note (*): A special adapter must be used for emulating this CPU.

You must configure jumpers J1 and J2 for CMOS or NMOS emulated CPU.

Note: The Emulator can emulate up to 16KB of CODE memory. Other memory (external CODE or XDATA) can not be accessed by the Emulator, it is however available to your program.
If you wish to debug external memory (CODE or XDATA) as well, use the 8031 POD instead. In that case the internal ROM contents should be downloaded.

Signal	Description
INT0-TINT0 INT1-TINT1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Caution: Since 80C154 is used on the POD, following registers / bits (available on 80C154) must not be used when 8051 CPU is emulated:

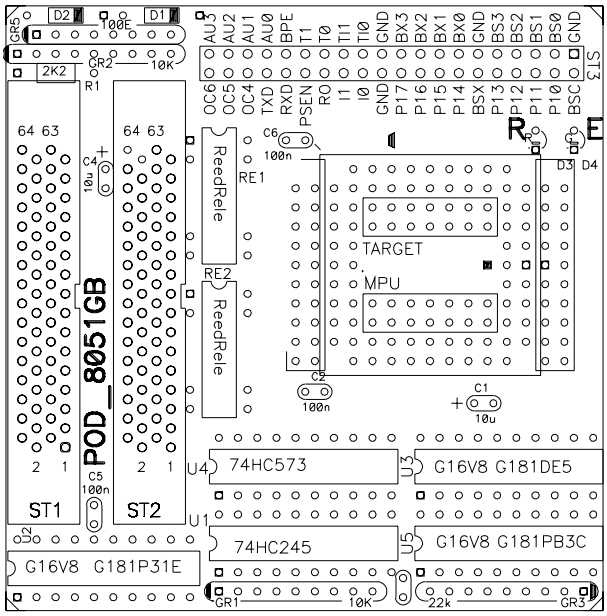
- IOCON (F8H)
- TH2 (CDH), TL2 (CCH)
- RCAP2H (CBH), RCAP2L (CAH)
- T2CON (C8H)
- IP (B8H) bit 5 (PT2, bit addr. BDh) and 7 (PCT, bit addr. BFh)
- IE (A8H) bit 5 (ET2, bit address ADH)
- PCON (87H) bit 5 (RPD) and 6 (HPD)

Intel 80C51GB POD rev. A

Ordering code	IC81030
POD Speed (MHz)	16
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	NO
Dimensions (mm)	79x80
Pin 1 position (mm)	72x46

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Target POD pinout is T_PLCC68 (See "T_PLCC68 POD Target Pinout" on page 583).

Emulated CPU
80C51 GB

Signal	Description
I0, TI0 I1, TI1	Bridge these pins to enable target interrupt
P1.0 - P1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32KB; Bridged=64KB
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32 KB; Bridged=64 KB
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

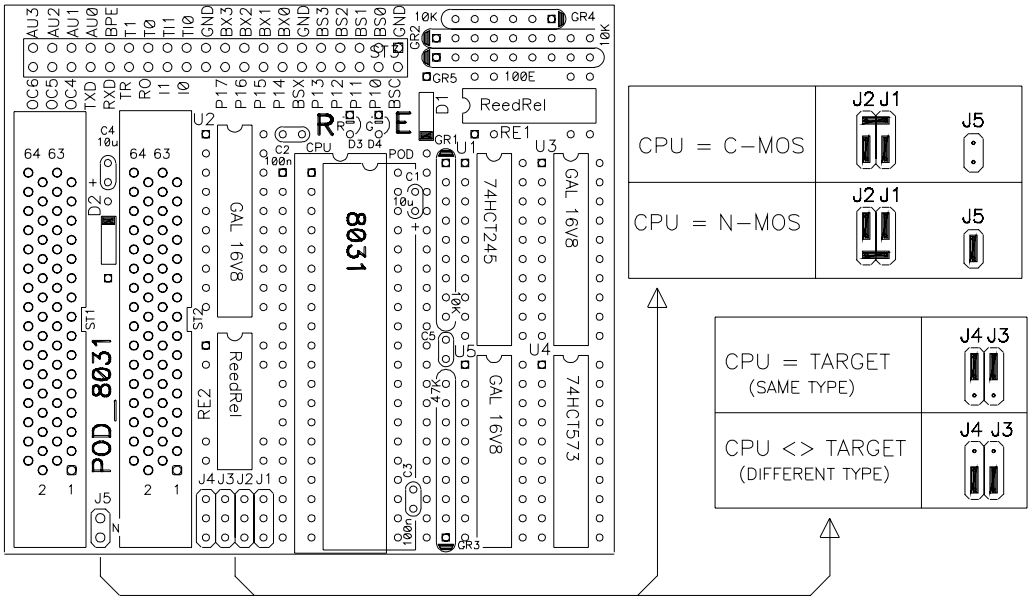
Dallas 80C320 POD rev. E, F, G

Ordering code	Discontinued (Was: IC81025)	
POD Speed (MHz)	21	25
Emulator Speed (ns)	90	65
Bank switch support	YES	
Exchange CPU	YES	
Dimensions (mm)	80x74	
Pin 1 position (mm)	41x52	

See "Intel 8051 Family – Standard PODs" on page 326.

This POD was discontinued and replaced with a new POD, that also supports the Dallas chips. See “Intel 8031/ Dallas 80320/ Infineon C504/ Philips 654/ Atmel 89S8252 POD rev. D” on page 337.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Target POD pinout is a standard DIP40.

Emulated CPU
DS 80C310
DS 80C320
DS 80C323

The pipeline nature of the Dallas 80C320 can sometimes lead to wrong XDATA breakpoint address identification. This is best shown in the example below:

```
MOV DPTR,#1000
MOVX @DPTR,A
MOV DPTR,#2000
```

If you set XDATA breakpoint on address 0x1000, program execution will break when this address is accessed, but since the CPU always fetches the next instruction before writing to XDATA, this instruction is executed as well. If this instruction modifies DPTR register, the wrong XDATA breakpoint address is reported. This may generate misleading notification messages (if the new DPTR address has a breakpoint set also), and inability to use pass counts and conditions with the breakpoint.

Jumper J1 determines the voltage level.

V_{CC} level	J1 setting
5.0 V	SET
3.3 V	CLEAR

Jumper J1 settings

The voltage setting must be done in the software as well.

Signal	Description
INT0-TINT0 INT1-TINT1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.
P1.0 - P1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32k; Bridged=64k
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32k; Bridged=64k
TXD, RXD	Transmit and receive lines for serial channel 0.

ST3 Connector signal description

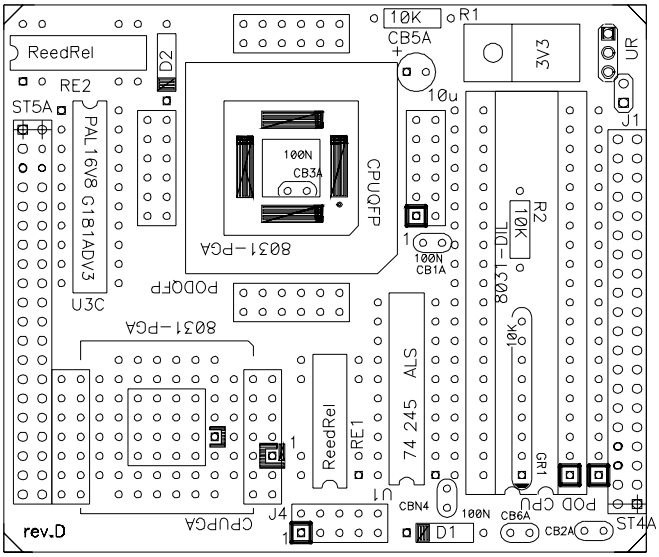
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Intel 8031/ Dallas 80320/ Infineon C504/ Philips 654/ Atmel 89S8252 POD rev. D

Ordering code	IC81025		
POD Speed (MHz) 8031	16	24	42
POD Speed (MHz) 80C320	/	21	25
Emulator Speed (ns)	150	90	65
Bank switch support	YES		
Exchange CPU	YES		
Dimensions (mm)	85x72		
Pin 1 position (mm)	DIL 79x10 PGA 35x13 QFP 54x44		

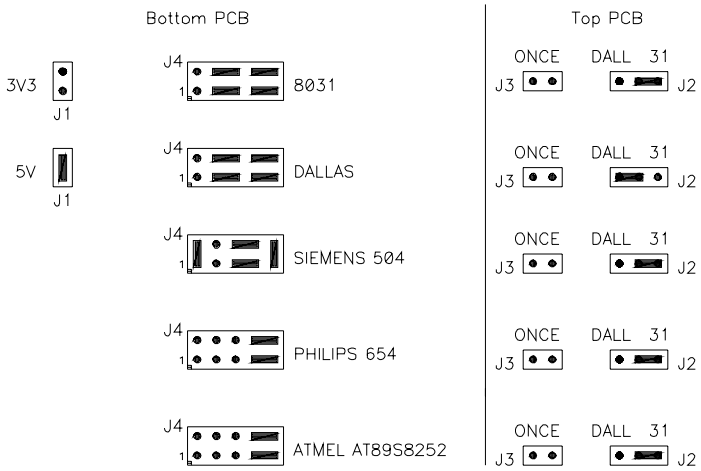
This POD is used with the universal 8051 POD motherboard (See "Intel 8051 Family – Standard PODs" on page 326).

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Bottom board

This POD combines can emulate numerous CPUs. The type of the POD/CPU is determined by jumper settings as follows:



Bottom board

Target POD pinouts:

- Standard DIP 40
- T_QFP44 (See "T_QFP44 POD Target Pinout" on page 584)
- T_PLCC44 (See "T_PLCC44 POD Target Pinout" on page 582)

Note: When configuring this POD in the "In-Circuit Emulation/CPU" dialog, you should always select the 8031 POD except when it is configured for Dallas CPUs. In this case select the DS80C320 POD.

Emulated CPU, 8031 mode
8031, 80C31 - 8032, 80C32
8051, 80C51 (*) - 8052, 80C52 (*)
83C44
80C154 (*)
80C851
80C410
SAB-C501, SAB-C502

Emulated CPU, DALLAS mode
DS 80C320
DS 80C310

Emulated CPU, Philips 654 mode
80C652
80C654

Emulated CPU, Infineon 504 mode
C504
C505
C505C

Emulated CPU, ATMEL AT89S8252 mode
80C8252

Jumper J1 determines voltage setting:

- 3.3 V when removed
- 5.0 V when set

Note: You must use the appropriate CPU (3.3 or 5V version) for the J1 setting.

Note: CPUs with internal ROM (*) can only be used if P0 and P1 CPU ports are available for external mode addressing. In such case program that resides in internal ROM must be downloaded.

This POD supports ONCE mode using a clip-over adapter. For this, the J3 jumper must be set.

Solder adapter:

- "DA44QFP(10*10)" on page 637

Signal	Description
P1.0 - P1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32k; Bridged=64k
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32k; Bridged=64k
BAN	No function

ST3 Connector signal description

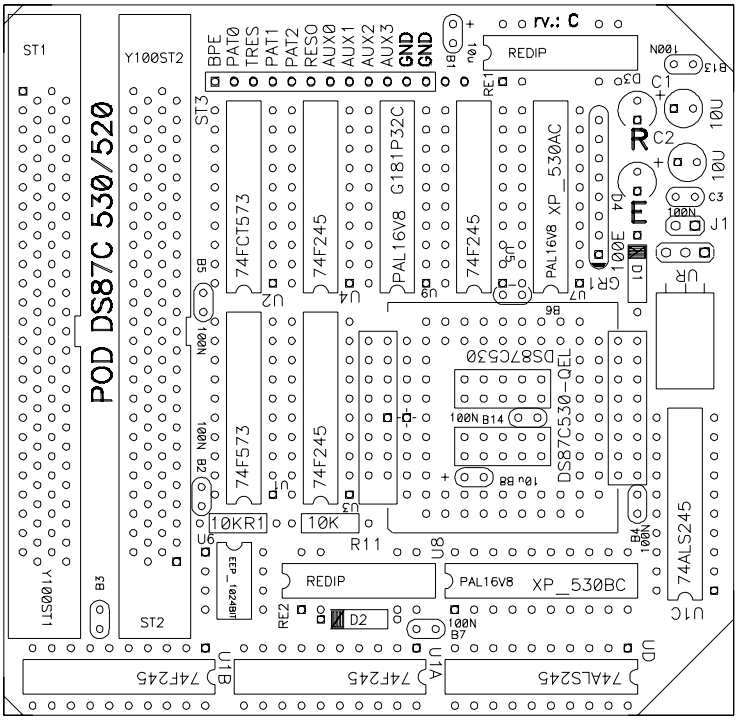
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Dallas 87C530 POD rev. C

Ordering code	IC20034	
POD Speed (MHz)	21	25
Emulator Speed (ns)	90	65
Bank switch support	NO	
Exchange CPU	NO	
Dimensions (mm)	97x94	
Pin 1 position (mm)	51x40	

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC1000 and the PowerEmulator unit. This POD can not be used with iC181.



Target POD pinout is T_PLCC52 (See "T_PLCC52 POD Target Pinout" on page 582).

Emulated CPU
DS 80C520
DS 80C530

The pipeline nature of the Dallas CPUs can sometimes lead to wrong XDATA breakpoint address identification. This is best shown in the example below:

```
MOV DPTR,#1000
MOVX @DPTR,A
MOV DPTR,#2000
```

If you set XDATA breakpoint on address 0x1000, program execution will break when this address is accessed, but since the CPU always fetches the next instruction before writing to XDATA, this instruction is executed as well. If this instruction modifies DPTR register, the wrong XDATA breakpoint address is reported. This may generate misleading notification messages (if the new DPTR address has a breakpoint set also), and inability to use pass counts and conditions with the breakpoint.

Note: This POD uses bondout chip which has 16K of internal memory enabled by default. If the internal ROM size should be minimized because of some special circumstances, different value should be writen in the protected ROMSIZE (RS2-0) register.

Example code for 'unlocking' the time protection and setting the ROM size to 8K:

```
mov 0C7H,#0AAH

mov 0C7H,#55H

mov 0C2H,#4H ; ROMSIZE register: 4 means romsize 8k
```

The complete code must be executed in running because time protection is unlocked for 3 CPU cycles only.

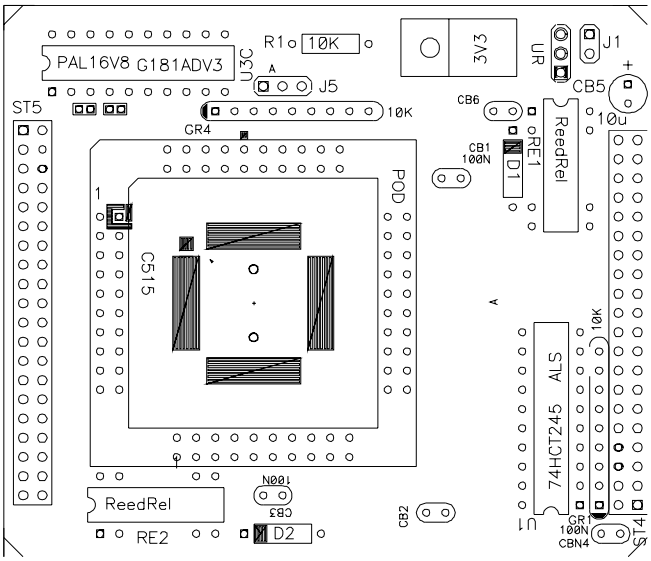
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon C515 POD rev. D

Ordering code	IC81033
POD Speed (MHz)	10
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	YES
Pin 1 position (mm)	15x45

This POD is used with the universal 8051 POD motherboard (See "Intel 8051 Family – Standard PODs" on page 326).

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU	J1 Position
C515C	A
C515A	A
C515	opposite A

Jumper J35 (on the bottom board) determines the voltage setting:

- 3.3 V when removed
- 5.0 V when set

Pin numbers on the target adapter correspond to pin numbers on the CPU. An additional adapter from the POD's target adapter to 80 QFP is optionally available.

Target POD pinout is T_QFP80 (See "T_QFP80 POD Target Pinout" on page 586).

Solder adapter: see "DA80QFP(14*14)" on page 639.

Signal	Description
I0-TI0 I1-TI1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
P1.0 - P1.7	Port P1 output pins. Can be used to connect with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32k; Bridged=64k
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32k; Bridged=64k
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

Note: The A/D converter works only when the POD is connected to the target. The reason is VA_REF and VA_GND that are connected only to the target adapter and therefore have no source - voltage reference, when POD operates without the target.

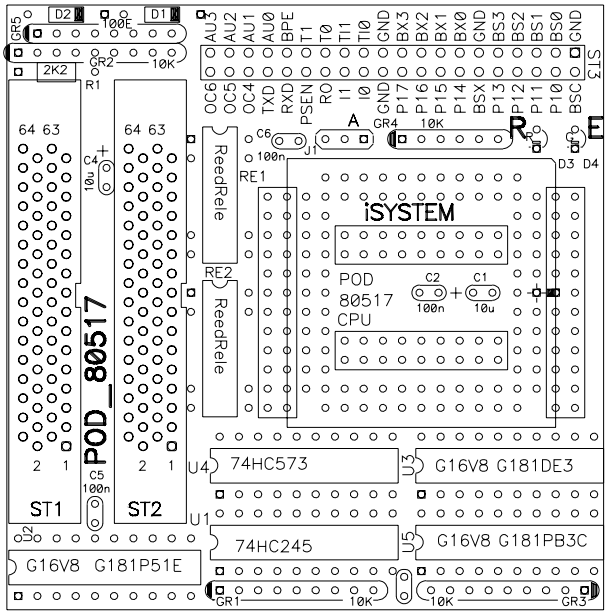
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon 80517 POD rev. C, D

Ordering code	IC81022
POD Speed (MHz)	18
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	YES
Dimensions (mm)	79x80
Pin 1 position (mm)	73x42

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



CPU = 517 = 535 = 535A	A J1
CPU = 517A	A J1

Target POD pinout is T_PLCC84 (See "T_PLCC84 POD Target Pinout" on page 584).

Emulated CPU	
80C535	80C515
80C537	80C517

Signal	Description
I0-TI0 I1-TI1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
P1.0 - P1.7	Port P1 output pins. Can be used to connect with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32k; Bridged=64k
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32k; Bridged=64k
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

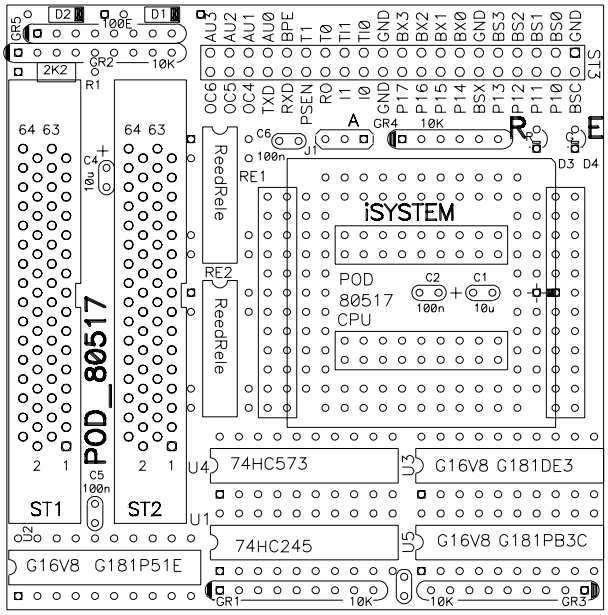
Note: Power Saving Mode pin (517A, 515A CPUs) is pulled low, thus disabling watchdog timer and enabling power saving mode. Since the Emulator does not support this mode, operations with PCON register that would cause the transition to power saving mode, are not allowed.

Infineon 80517A POD rev. C, D

Ordering code	IC81024-18
POD Speed (MHz)	18
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	YES
Dimensions (mm)	79x80
Pin 1 position (mm)	73x42

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



CPU = 517 = 535 = 535A	A J1
CPU = 517A	A J1

Target POD pinout is T_PLCC84 (See "T_PLCC84 POD Target Pinout" on page 584).

Emulated CPU	
80C515A	83C515A
80C517A	83C517A

Signal	Description
I0-TI0 I1-TI1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
P1.0 - P1.7	Port P1 output pins. Can be used to connect with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32k; Bridged=64k
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32k; Bridged=64k
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

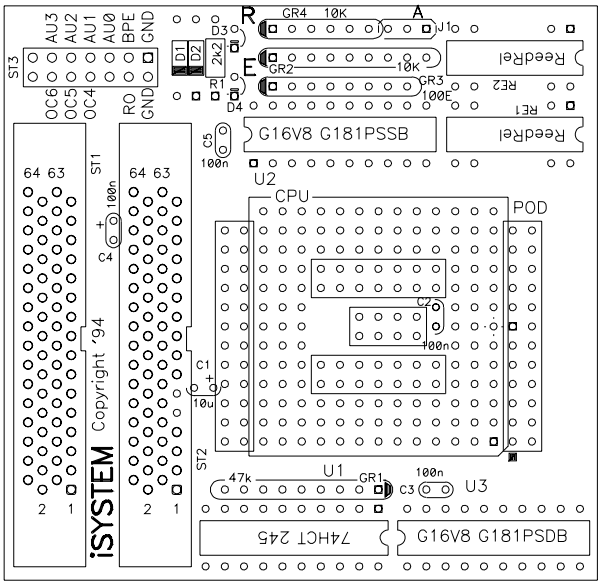
Note: Power Saving Mode pin (517A, 515A CPUs) is pulled low, thus disabling watchdog timer and enabling power saving mode. Since the Emulator does not support this mode, operations with PCON register that would cause the transition to power saving mode, are not allowed.

Infineon 80517-B POD rev. A, B

Ordering code	IC81027
POD Speed (MHz)	16
Emulator Speed (ns)	90
Bank switch support	NO
Exchange CPU	NO
Dimensions (mm)	78x75
Pin 1 position (mm)	66x33

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU	
80C535	80C515
80C537	80C517

Target POD pinout is T_PLCC84 (See "T_PLCC84 POD Target Pinout" on page 584).

For 80C515 and 80C535 a special socket adapter must be used. If you wish to emulate internal ROM, the program that resides in it must be downloaded.

Note: If you are using XDATA with this POD it can only be used (and mapped) from the target.

Signal	Description
I0-TI0 I1-TI1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

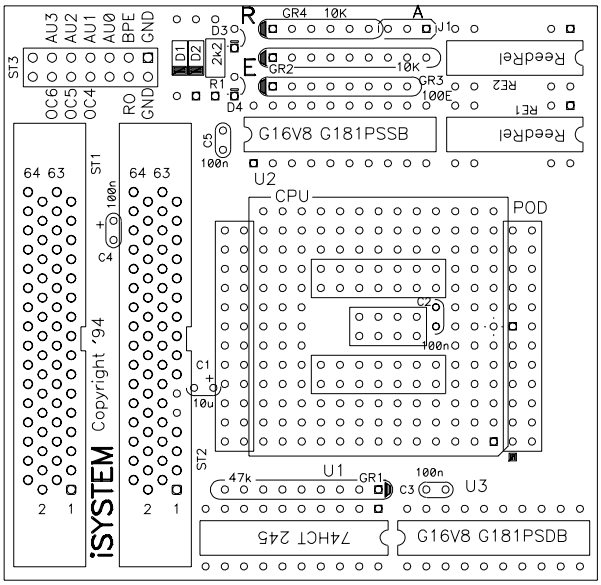
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon 80517A-B POD rev. A, B

Ordering code	IC81028
POD Speed (MHz)	18
Emulator Speed (ns)	90
Bank switch support	NO
Exchange CPU	NO
Dimensions (mm)	78x75
Pin 1 position (mm)	66x33

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU	
80C515A	83C515A
80C517A	83C517A

Target POD pinout is T_PLCC84 (See "T_PLCC84 POD Target Pinout" on page 584).

For 83C515A and 80C515A a special socket adapter must be used. If you wish to emulate internal ROM, the program that resides in it must be downloaded.

Note: If you are using XDATA with this POD it can only be used (and mapped) from the target.

Signal	Description
I0-TI0 I1-TI1	Bridge these pins to enable target interrupt
IC1 - IC3	Reserved for later use
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

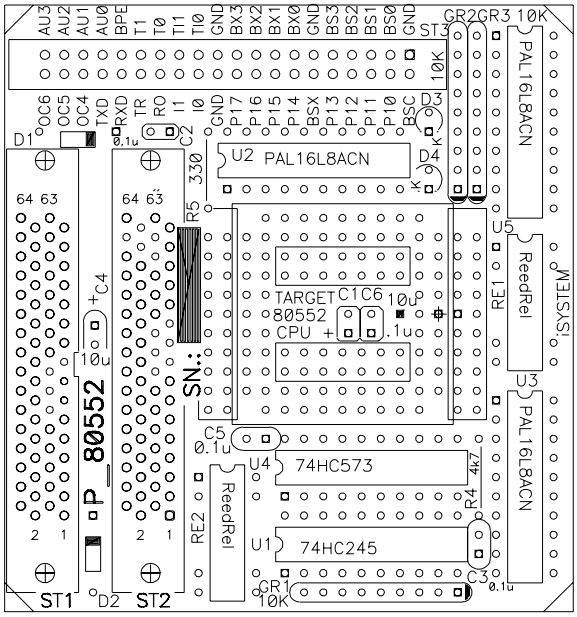
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Philips 80552 POD rev. A, B, D

Ordering code	IC81023	
POD Speed (MHz)	16	30
Emulator Speed (ns)	90	90
Bank switch support	YES	
Exchange CPU	YES	
Dimensions (mm)	75x80	
Pin 1 position (mm)	60x39	

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
80C552
80C554
80C562

Target POD pinout is T_PLCC68 (See "T_PLCC68 POD Target Pinout" on page 583)

Signal	Description
I0, TI0 I1, TI1	Bridge these pins to enable target interrupt
P1.0 - P1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32 KB; Bridged=64 KB
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32 KB; Bridged=64 KB
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

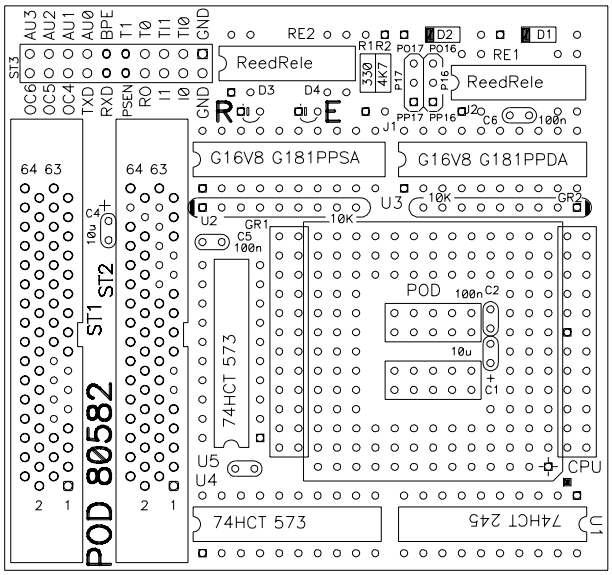
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Philips 83C552-B POD rev. A, B

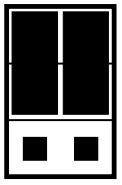
Ordering code	IC81026
POD Speed (MHz)	24
Emulator Speed (ns)	90
Bank switch support	NO
Exchange CPU	NO
Dimensions (mm)	79x74
Pin 1 position (mm)	69x15

See "Intel 8051 Family – Standard PODs" on page 326.

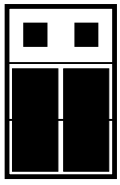
This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU	Adapter	PP16, PP17 setting (*)
80C552, 83C552, 87C552	68 PGA	OD
83C552+EEPROM	68 PGA	OD
80C652, 83C652, 87C652	40 DIL	OD
80C652+EEPROM	40 DIL	OD
80C51BH	40 DIL	PP
83C851	40 DIL	PP
80C562, 83C562	68 PGA	PP
83C662	40 DIL	PP



PP(Push-Pull)

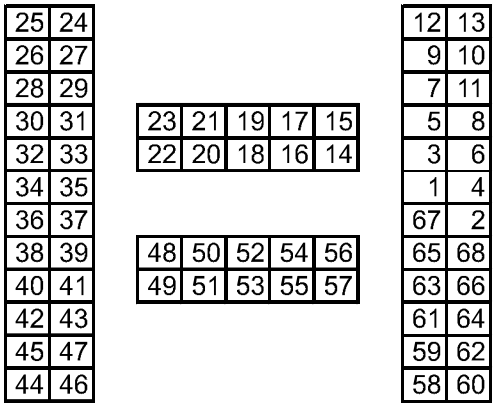


OD (Open Drain)

PP16, PP17 jumper settings

Note: Other 8051 derivatives can be used, if the desired CPU's SFRs are a subset of one of the listed CPUs and the internal RAM size is large enough.

Target POD pinout is PLCC68.



Target POD pinout

Applications using internal ROM, external ROM, external RAM and all combinations are supported without limitations. Also the EA input from target is correctly interpreted.

The bondout chip, used as the emulation CPU, can suspend following the CPU activities when the CPU is stopped (configurable from the CPU setup dialog):

- Timer0, Timer1 and Timer2 operation
- New interrupt generation (from any source)
- Stop the UART unless it is in shift register mode. If the UART port is in the shift register mode and is in the middle of sending or receiving a byte, it will finish the current byte then stop. Data will be lost if the UART port is in the asynchronous mode and INTD occurs while it is sending or receiving.

The following settings must be configured correctly so that the POD can operate as the selected CPU in the target system:

- CPU type. According to this selection CPU specific special purpose registers are available and internal RAM size is determined.
- internal ROM size 4, 8, 16 or 32 Kbytes. If internal ROM is used (EA=1), then addressing CODE memory above this size will lead to external EPROM addressing. This selection is not CPU type specific, thus you can use more CODE memory when you develop your application, than when the CPU is programmed. See also Memory mapping.

Signal	Description
I0, TI0 I1, TI1	Bridge these pins to enable target interrupt
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

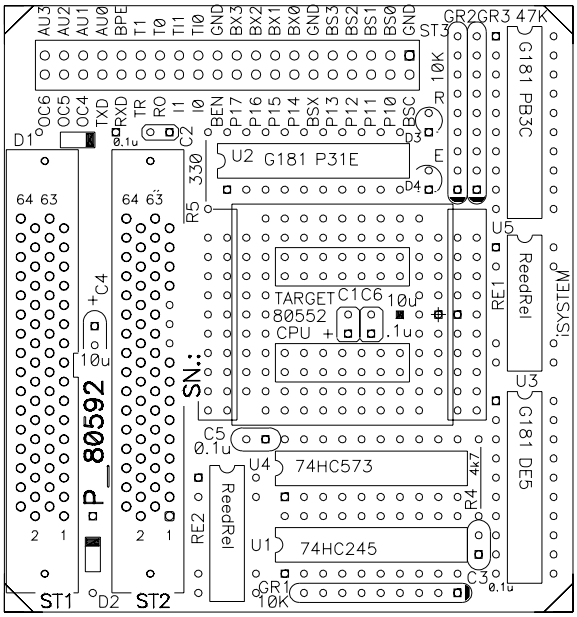
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Philips 80C592 POD rev. A

Ordering code	IC81029
POD Speed (MHz)	16
Emulator Speed (ns)	90
Bank switch support	YES
Dimensions (mm)	75x80
Pin 1 position (mm)	60x40

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
80C592

Target POD pinout is T_PLCC68 (See "T_PLCC68 POD Target Pinout" on page 583).

Note: The 80592 CPU contains the first 256 bytes of XDATA memory. Since no external addresses are generated when accessing this area, no address breakpoints or tracing this memory region is available.

Signal	Description
I0, TI0 I1, TI1	Bridge these pins to enable target interrupt
P1.0 - P1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 – BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32KB; Bridged=64KB
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32 KB; Bridged=64KB
TXD, RXD	Transmit and receive lines for serial channel 0.
T0, T1	Timer outputs T0 and T1.

ST3 Connector signal description

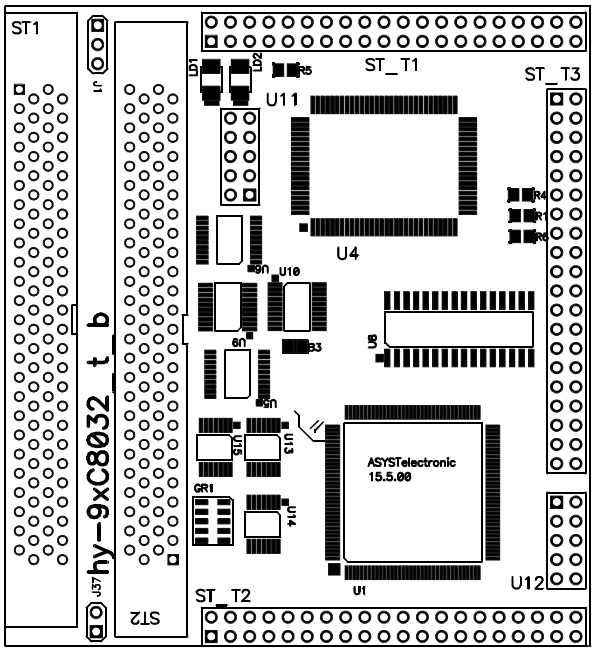
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Hyundai HMS9XC8032 POD rev. B

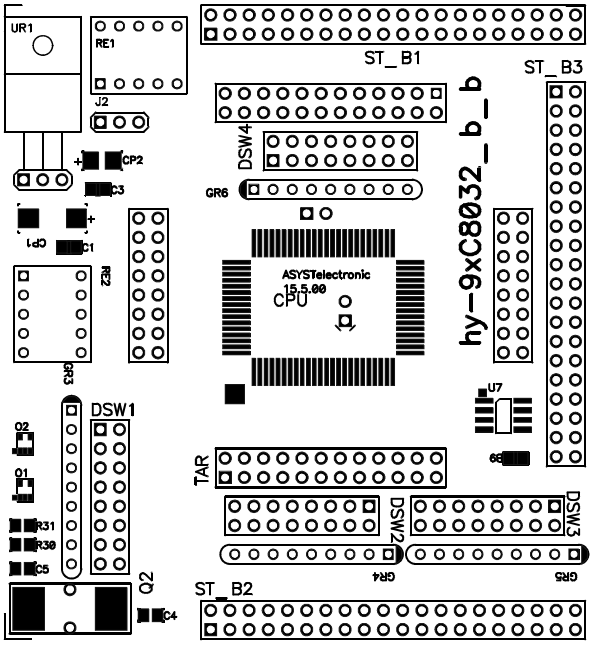
Ordering code	IC10100
POD Speed (MHz)	7.2
Emulator Speed (ns)	90
Bank switch support	NO
Top Board Dimensions (mm)	77.5x85
Bottom Board Dimensions (mm)	77x84
Pin 1 position (mm)	29x21.5

See "Intel 8051 Family – Standard PODs" on page 326.

This POD can be used on iC1000 and the PowerEmulator unit.



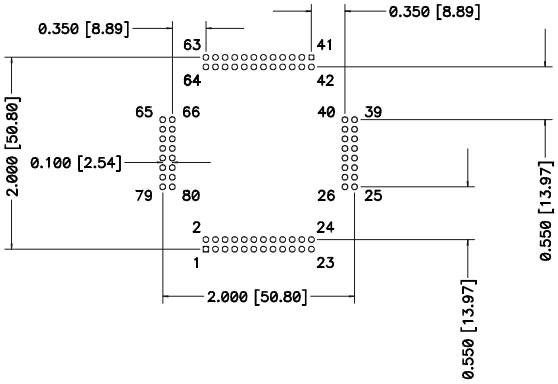
Top board



Bottom board

Emulated CPU
HMS9XC8032

Target POD pinout is IA80QFP1420.



Target POD pinout

Jumper J2 selects the CPU voltage when Emulator is the supply source.

CPU Voltage (Emulator)	Jumper J2 Setting
3.3 V	1-2
5 V	2-3

There is a number of jumpers to set the Pull-up resistors for ports P0, P1, P2 and P6. All these are the ports, implemented on the POD with port replacement. There are four groups of jumpers installed:

- jumpers marked DSW1 set the Pull-up for port P0
- jumpers marked DSW2 set the Pull-up for port P1
- jumpers marked DSW3 set the Pull-up for port P2
- jumpers marked DSW4 set the Pull-up for port P6

The label of jumpers on the POD is always located next to the MSB bit of the port, i.e. the label DSW1 is located next to P0.7, the port P0.0 is located on the opposite side.

A U11 connector is located on the POD.

2	4	6	8	10
GND	AUX0	AUX1	AUX2	AUX3
GND	GND	BPEXT	RESO	TRESET
1	3	5	7	9

U11 Connector signal pinout

Signal	Description
BPEXT	External Breakpoint
RESO	Reset Output
TRESET	Target Reset
AUX0..3	Auxilliary inputs

U11 Connector signal description

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Intel 8051 Family – Infineon E-Hooks PODs

All 8051 family PODs are 8-bit PODs that can be used on iC181, iC1000 and the PowerEmulator unit with the exception of a few PODs, that can not be used on the iC181 unit. Please check the description of the POD if you want to use it with the iC181 Emulator.

Bank switching is supported on non-single chip PODs.

See "In-Circuit Emulation PODs" on page 324 for general POD information.

Before connecting the PODs, make sure you have read the technical notes on "Intel 8051 Family" on page 145.

The following Infineon Enhanced Hooks PODs are described in this part of the manual, in order of appearance:

Note: Always use (exchange) the appropriate CPU in the POD.

Setting CPU options

The **Operating Mode** (see "Advanced In-Circuit Emulation Options (8051)" on page 145) must be selected. The POD will always operate in the mode selected in software – the target EA is ignored.

If the **External XDATA enabled** option (see "Advanced In-Circuit Emulation Options (8051)" on page 145) is set, the CPU will generate an external cycle (P0, P2, RD and WR) every time a MOVX instruction is executed.
In a single chip application where only the internal XDATA memory is used and P0 and P2 are used by the application, this option must be disabled.

The **Stop CPU Activities when Stopped** option (see "CPU Options" on page 42) is functional only in **Single Chip** mode.

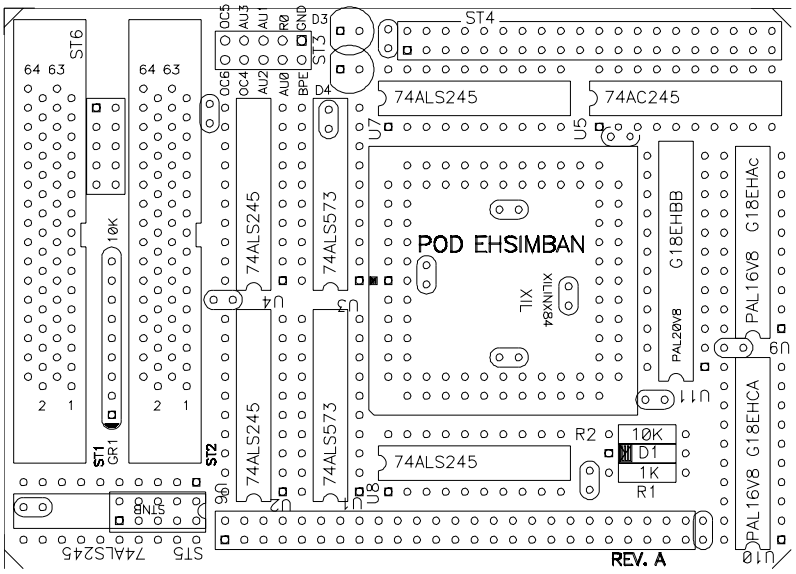
Also note following differences between standalone CPU and POD operation:

- 10k pull-down or pull-up at RESET input, depending on active RESET level – pulling away from RESET.
- P0 is reconstructed by Xilinx. It works as 'open drain output' without pull-up logically the same as CPU. Input level is TTL
- P2 is reconstructed by Xilinx. It works as 'open drain output' with 1k pull-up logically the same as CPU. Input level is TTL. The 1k pull-up is used because of some timing reasons when using in extended mode. The pull-up resistors are installed in a socket, therefore if required, the resistors can be replaced with a higher value. Using the resistors of more than 10k is not advisable, since this could drastically increase the time needed for a switch from logic state 0 to 1, which would cause timing problems in the target.
- PSEN, ALE are reconstructed by a GAL. Output levels can be a little bit different - but still TTL.

Infineon EH-C500 POD Motherboard rev A

Dimensions (mm)	104x74

This motherboard POD is used as a top board for all Infineon EH-C500 PODs.

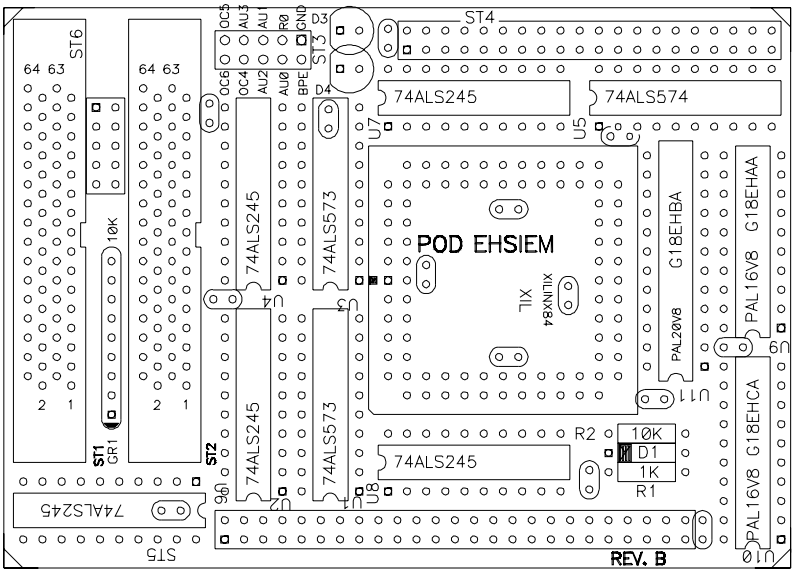


Top board

Infineon EH-C500 POD Motherboard rev B

Dimensions (mm)	104x74

This motherboard POD is used as a top board for all Infineon EH-C500 PODs.



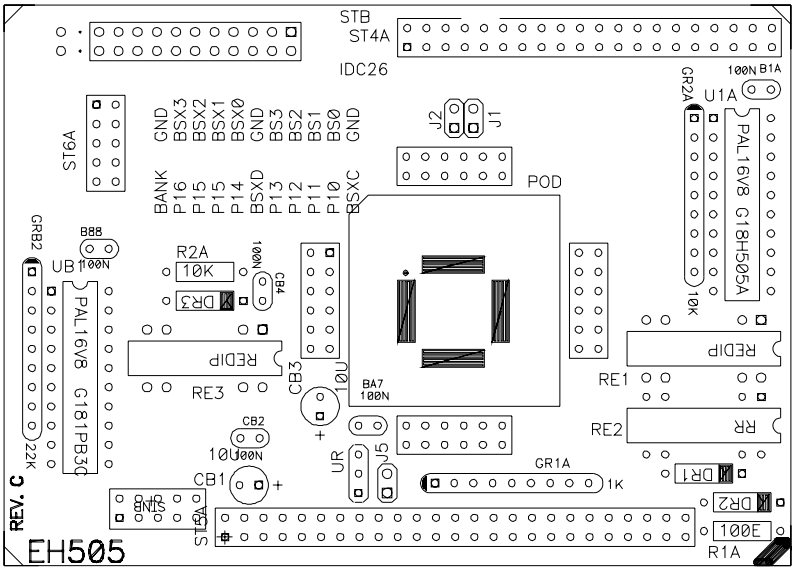
Top board

Infineon EH-C505 POD rev. C

Ordering code	IC81500	
POD Speed (MHz)	40/20	33/16
Emulator Speed (ns)	65	90
Bank switch support	YES	
Exchange CPU	YES	
Pin 1 position (mm)	43x41	

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU	
C504	(40/33 MHz)
C505	(20/16 MHz)
C505A	(20/16 MHz)
C505C	(20/16 MHz)
C505CA	(20/16 MHz)

Target POD pinout is T_QFP44 (See "T_QFP44 POD Target Pinout" on page 584).

If AD converter operation is desired when the POD is used standalone (without target), VAREF can be connected to VCC with jumper J1 and VAGND to GND with jumper J2.

Note: If POD is used in the target, jumpers J1 and J2 must be removed, otherwise a short between target and Emulator Vcc will occur.

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

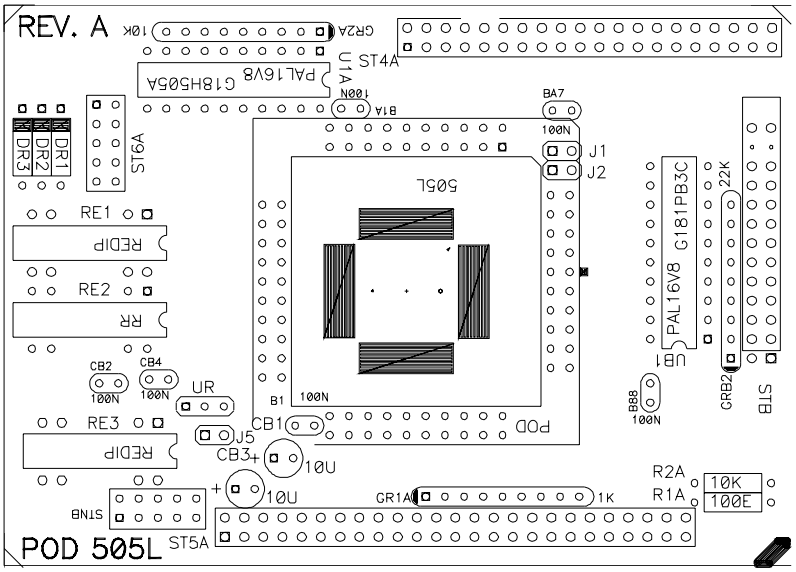
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C505L POD rev. A

Ordering code	IC81505	
POD Speed (MHz)	20	16
Emulator Speed (ns)	65	90
Bank switch support	YES	
Exchange CPU	NO	
Pin 1 position (mm)	66x56	

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
C505L

Target POD pinout is T_QFP80 (See "T_QFP80 POD Target Pinout" on page 586).

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

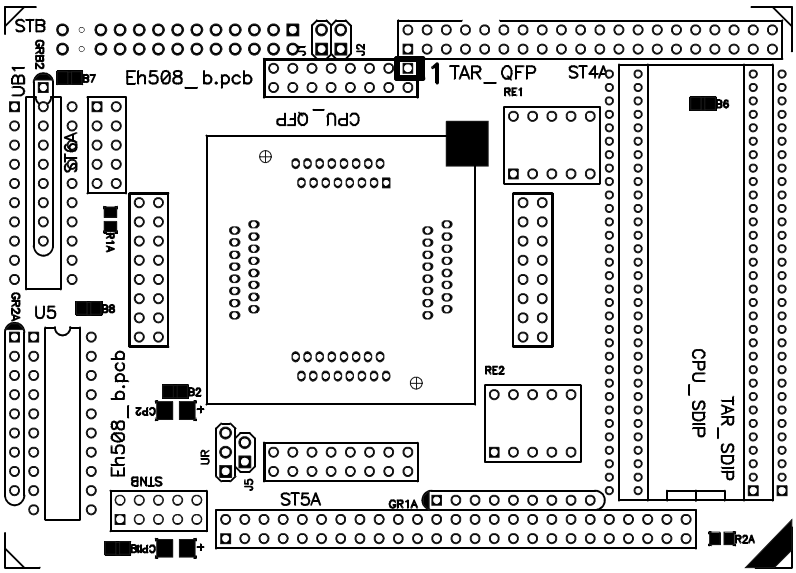
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C508 POD rev. B

Ordering code	IC81507	
POD Speed (MHz)	16	20
Emulator Speed (ns)	90	65
Bank switch support	YES	
Exchange CPU	NO	
Dimensions (mm)	104x75	
Pin 1 position (mm)	53x66 (QFP) 102x11 (SDIP)	

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
C508

Jumper selector J1 allows connecting VAREF and VAGND voltages for the A/D converter. These jumpers should be set when POD is operated standalone (without target) and removed when target reference and GND should be used.

Jumper J5 determines the Vcc voltage level.

Position	Vcc level
Set	5.0 V
Removed	3.3 V

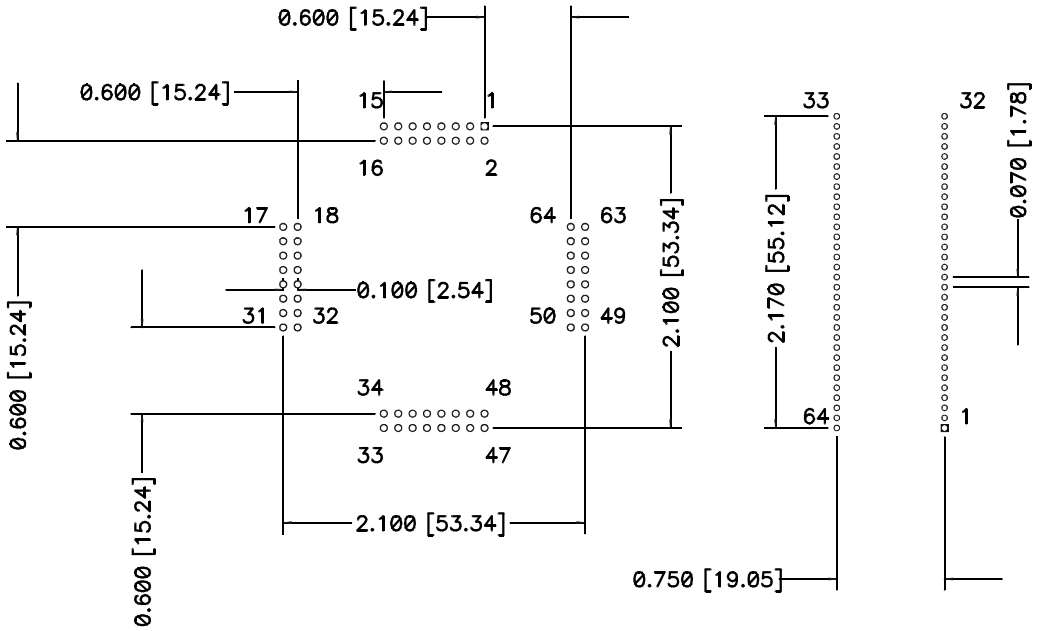
Jumper J5 settings

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Target POD pinout is a standard SDIP64 and T_QFP64, as shown in the picture below.



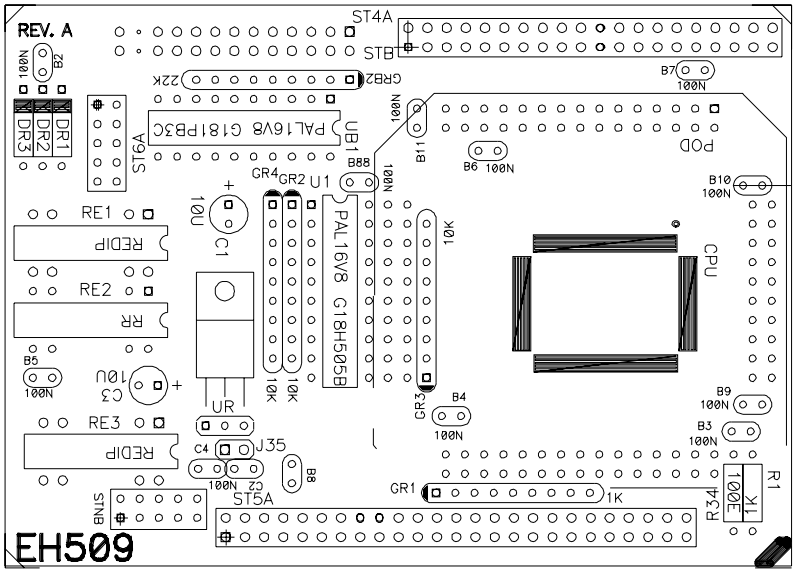
Target POD pinout

Infineon EH-C509 POD rev. A

Ordering code	IC81506
POD Speed (MHz)	16
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	NO
Pin 1 position (mm)	66x33

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
C509

Target POD pinout is T_QFP100 (See "T_QFP100 POD Target Pinout" on page 587).

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

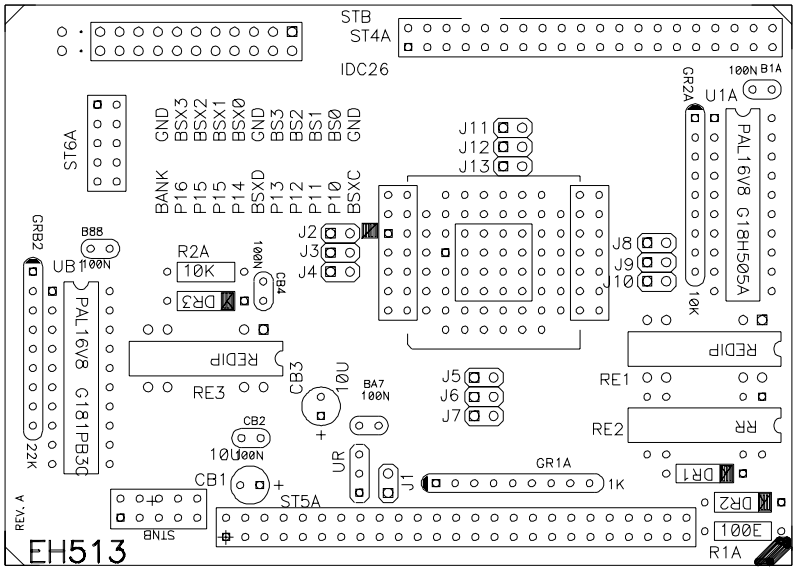
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C513 POD rev. A

Ordering code	IC81503
POD Speed (MHz)	12/16
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	YES
Pin 1 position (mm)	50x44

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
C501G
C513
C513A
C513A0
C511
C511A

Target POD pinout is T_PLCC44 (See "T_PLCC44 POD Target Pinout" on page 582).

Jumper J1 selects V_{CC} voltage level

V_{CC} level	J1 setting
5.0 V	SET
3.3 V	CLEAR

Jumper J1 settings

The table below gives shows where CPU pins 1, 12, 23 and 34 are connected depending on jumper J2 through J13 setting.

	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13
CPU pin	1	1	1	12	12	12	23	23	23	34	34	34
Target pin	X			X			X			X		
GND		X			X			X			X	
Vcc			X			X			X			X

The table below indicates which jumpers must be set for the CPU emulated.

CPU	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13
C501G	SET			SET			SET			SET		
C513	SET			SET			SET			SET		
C513A	SET			SET			SET			SET		
C513A0		SET		SET					SET	SET		
C511	SET			SET			SET			SET		
C511A	SET			SET			SET			SET		

Note: always configure jumpers according to the CPU used.

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

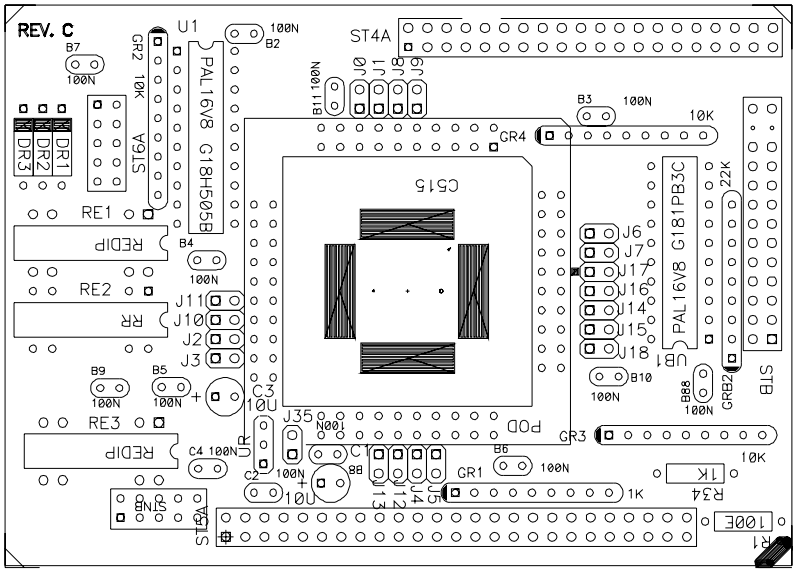
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C515 POD rev. C

Ordering code	IC81501
POD Speed (MHz)	24/10
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	YES
Pin 1 position (mm)	65x55

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU	J0 J1	J2 J3	J4 J5	J6 J7	J8 J9	J10 J11	J12 J13	J14 J15	J16 J17	J18
CPU pin	13	35	51	70	14	32	50	68	69	69
C515 (24MHz)	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
C515A (24MHz)	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
C515B (24MHz)										
C515C (10MHz)	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF

Note: always configure jumpers according to the CPU used.

Target POD pinout is T_QFP80 (See "T_QFP80 POD Target Pinout" on page 586).

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

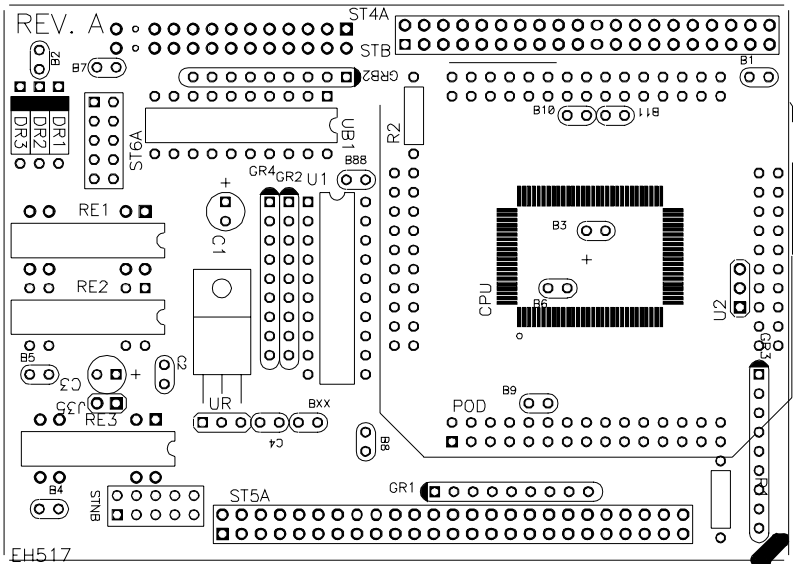
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C517 POD rev. A

Ordering code	IC81504
POD Speed (MHz)	24
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	NO
Pin 1 position (mm)	58.5x15

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Emulated CPU
C517A

Target POD pinout is T_QFP100 (See "T_QFP100 POD Target Pinout" on page 587).

Jumper J35 selects V_{CC} voltage level

V_{CC} level	J1 setting
5.0 V	SET
3.3 V	CLEAR

Jumper J35 settings

Signal	Description
BS0 – BS3	Bank select lines for CODE memory banking.
BSXC	CODE Bank size select. Open<=32k; Bridged=64k
BSXD	XDATA Bank size selct. Open<=32k; Bridged=64k
P10 – P17	Port P1 output pins. Can be used in connection with BS0-BS3 and BSX0-BSX3 pins for bank switching through port P1.
BSX0 – BSX3	Timer outputs T0 and T1.

STB Connector signal description

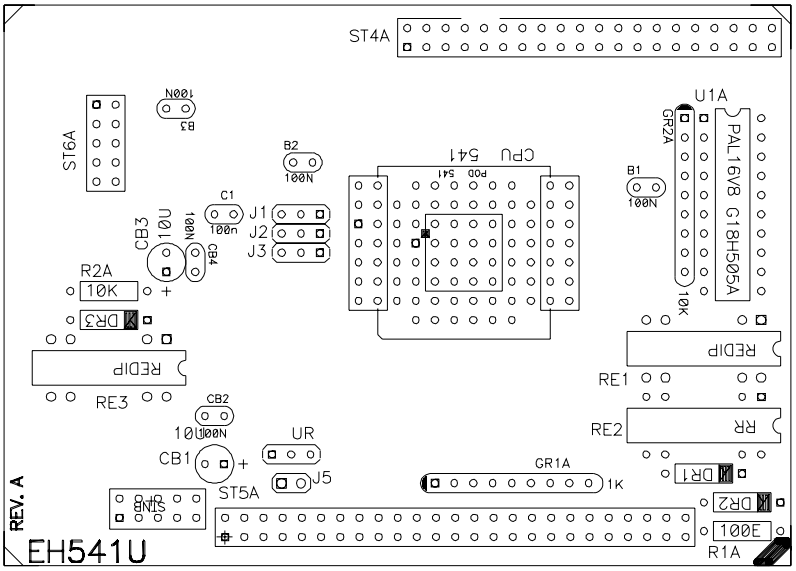
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C541U POD rev. A

Ordering code	IC81502
POD Speed (MHz)	12
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	NO
Pin 1 position (mm)	66x33

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Target POD pinout is T_PLCC44 (See "T_PLCC44 POD Target Pinout" on page 582).

Emulated CPU
C540U
C541U

Jumpers J1-J3 define the following (pin 1 is located next to the CPU).

Jumper J1 selects V_{CCU} source

V_{CCU} source	J1 setting
Target	1-2
Emulator (CPU)	2-3

Jumper J1 settings

Jumper J2 selects CPU revision

Revision	J2 setting
Prior to CA	1-2
CA or later	2-3

Jumper J2 settings

Jumper J3 selects V_{SSU} source

V_{SSU} source	J3 setting
Target	1-2
GND	2-3

Jumper J3 settings

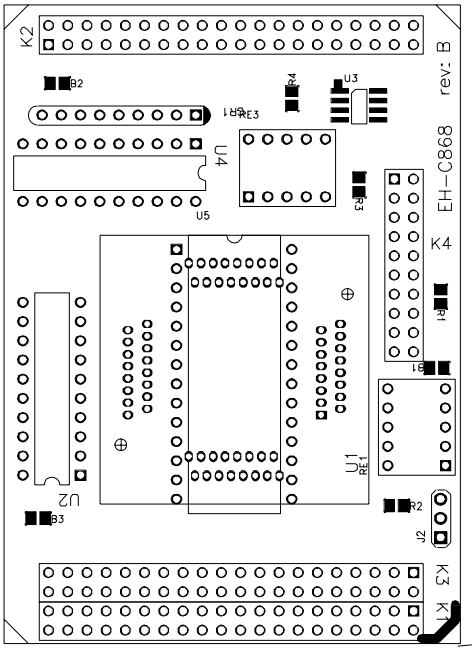
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-C868 POD rev. B

Ordering code	IC81800
POD Speed (MHz)	40/10
Emulator Speed (ns)	65
Bank switch support	NO
Exchange CPU	NO
Dimensions (mm)	60.5x84.5
Pin 1 position (mm)	23x52

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC1000 and the PowerEmulator unit. It can not be used with iC181.



Target POD pinout is DIL28.

Emulated CPU
C868

Jumper J2 selects Emulator V_{CC} level

V_{CC} level	J2 setting
3.3 V	1-2
5.0 V	2-3

Jumper J2 settings

Note: POD supports only single chip operation

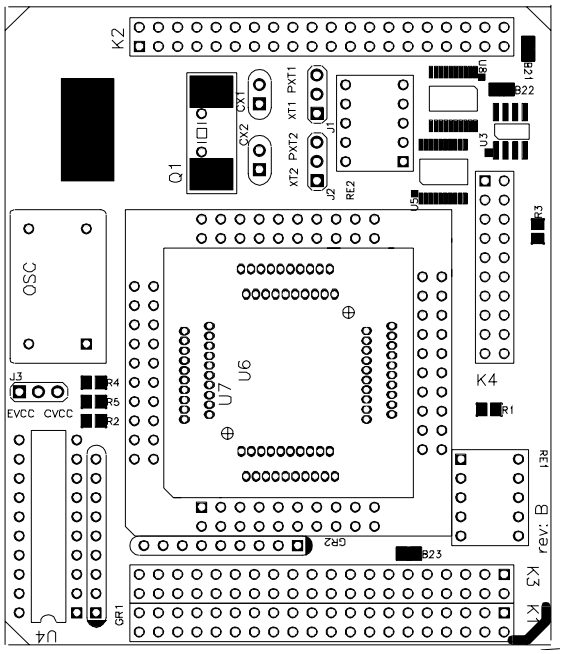
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Infineon EH-PSB2154 POD rev. B

Ordering code	IC81820
POD Speed (MHz)	48/7.68
Emulator Speed (ns)	65
Bank switch support	NO
Exchange CPU	NO
Dimensions (mm)	72x84.5
Pin 1 position (mm)	26x18.5

See "Intel 8051 Family – Infineon E-Hooks PODs" on page 363.

This POD can be used on iC1000 and the PowerEmulator unit. It can not be used with iC181.



Target POD pinout is T_QFP80 (See "T_QFP80 POD Target Pinout" on page 586).

Solder adapter: see "DA80QFP(14*14)" on page 639

Emulated CPU
PSB2154

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

An oscillator or a quartz can be installed in this POD. This means that this POD can operate with three different clock types:

1) Emulator Clock;
2) Target Clock;
3) POD Clock.

If ‘Emulator Clock’ is selected in the software, with jumpers J1 and J2 it is selected whether Emulator clock (PLL) or quartz or oscillator on the POD will be used.

J1 setting	Description
XT1	Emulator clock
PXT1	Oscillator or quartz on the POD

Jumper J1 settings

J2 setting	Description
XT2	Emulator clock
PXT2	Oscillator or quartz on the POD

Jumper J2 settings

If the clock from the POD is selected, either the oscillator or the quartz can be used (only one at a time).

The oscillator can be inserted into the OSC_DIP14 socket. The required volage of the oscillator is set using jumper J3.

J3 setting	Voltage
EVCC	5V (Emulator VCC)
CVCC	3V3 (CPU power supply)

Jumper J3 settings

The quartz can be inserted into the Q1 socket. Capacitors, connected to XTAL1 and XTAL2 on the CPU, must be inserted into the CX1 and CX2 sockets.

Note: As a CPU limitation, the Read Modify Write instructions do not operate on port P0.

Intel 8051 Family – Philips Hooks PODs

All 8051 family PODs are 8-bit PODs that can be used on iC181, iC1000 and the PowerEmulator unit with the exception of a few PODs, that can not be used on the iC181 unit. Please check the description of the POD if you want to use it with the iC181 Emulator.

Bank switching is supported on non-single chip PODs.

See "In-Circuit Emulation PODs" on page 324 for general POD information.

Before connecting the PODs, make sure you have read the technical notes on "Intel 8051 Family" on page 145.

The following Philips Hooks PODs are described in this part of the manual, in order of appearance:

Note: Always use (exchange) the appropriate CPU in the POD.

Setting CPU options

The **Operating Mode** (see “Advanced In-Circuit Emulation Options (8051)” on page 145) must be selected. The POD will always operate in the mode selected in software – the target EA is ignored.

If the **External XDATA enabled** option (see “Advanced In-Circuit Emulation Options (8051)” on page 145) is set, the CPU will generate an external cycle (P0, P2, RD and WR) every time a MOVX instruction is executed.
In a single chip application where only the internal XDATA memory is used and P0 and P2 are used by the application, this option must be disabled.

The **Stop CPU Activities when Stopped** option (see “CPU Options” on page 42) is functional only in **Single Chip** mode.

Also note following differences between standalone CPU and POD operation:

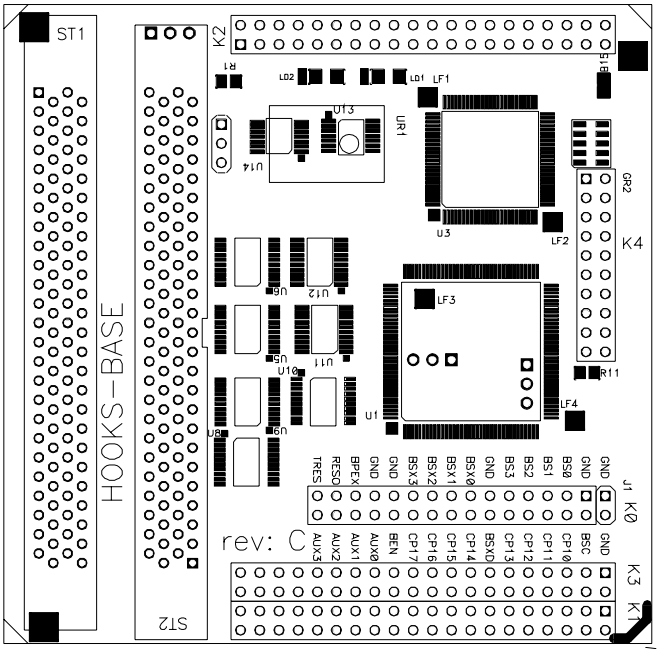
- 10k pull-down or pull-up at RESET input, depending on active RESET level – pulling away from RESET.
- P0 is reconstructed by Xilinx. It works as 'open drain output' without pull-up logically the same as CPU. Input level is TTL

- P2 is reconstructed by Xilinx. It works as 'open drain output' with 1k pull-up logically the same as CPU. Input level is TTL. The 1k pull-up is used because of some timing reasons when using in extended mode. The pull-up resistors are installed in a socket, therefore if required, the resistors can be replaced with a higher value. Using the resistors of more than 10k is not advisable, since this could drastically increase the time needed for a switch from logic state 0 to 1, which would cause timing problems in the target.
- PSEN, ALE are reconstructed by a GAL. Output levels can be a little bit different - but still TTL.

Hooks POD Motherboard rev C

Dimensions (mm)	104x74

This motherboard POD is used as a top board on some hooks PODs.



Top board

Signal	Description
CP1.0 – CP1.7	Port P1 output pins. Can be used in connection with BS0 - BS3 and BX0 - BX3 pins for bank switching through port P1.
BS0 - BS3	Bank select lines for CODE memory banking.
BSC	CODE Bank size select. Open<=32 KB; Bridged=64 KB
BX0 - BX3	Bank select lines for XDATA memory banking.
BSX	XDATA Bank size select. Open<=32 KB; Bridged=64 KB

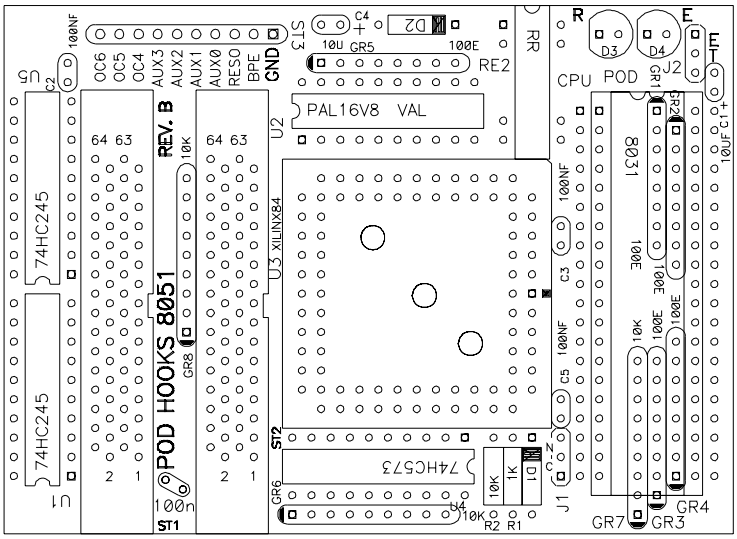
K0 Connector signal description

Philips 8052 Hooks POD rev. B

Ordering code	IC81031
POD Speed (MHz)	16
Emulator Speed (ns)	90
Bank switch support	NO
Exchange CPU	YES
Dimensions (mm)	96x70
Pin 1 position (mm)	79x56

See "Intel 8051 Family – Philips Hooks PODs" on page 387.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Target POD pinout is a standard DIP40.

Emulated CPU
80C51
80C31
8xC52
8xC32
80C52
80C54
80C58
8xC053
8xC054
8xC51 FA, FB, FC
8xC51 RA, RB, RC, RD
8xC51 RA+, RB+, RC+, RD+
8xC504
8xC524
8xC528
8xC550
8xC575
8xC652
8xC654
AT89Cx051

Note: You must always exchange the CPU on the POD with a Signetics/Philips equivalent (with built-in support for hooks mode emulation). The only exception is the 80C51/80C31, where an 80C32 CPU must be used.

CPU	Position
NMOS	N
CMOS	C

Jumper J1 CMOS/NMOS settings

This POD uses a special emulation mode (hooks mode) to emulate the CPU. As a consequence, ports P0 and P2 are emulated with on POD XILINX CPLD (type XC3190A) resulting in slightly different AC and DC characteristics to the original CPU.
Both ports and ALE and PSEN lines have serial 100-ohm resistors for protection; P2 has additional 10k pull-ups on the target side.

Note: As clock source a standalone clock must always be used, either internal or external from the target. The Clock signal is not directly connected to the CPU pin because the clock signal is required for HOOKS mode implementation. Thus when external clock is selected, the oscillator must be used in the target and not the crystal which would not oscillate at all since it's not connected directly to the CPU pin.

Vcc source on this POD is configured via J2 jumper:

Source	Position
Emulator	E
Target	T

Jumper J2 Vcc Source settings

Note: Jumpers can only be changed when the Emulator is switched off.

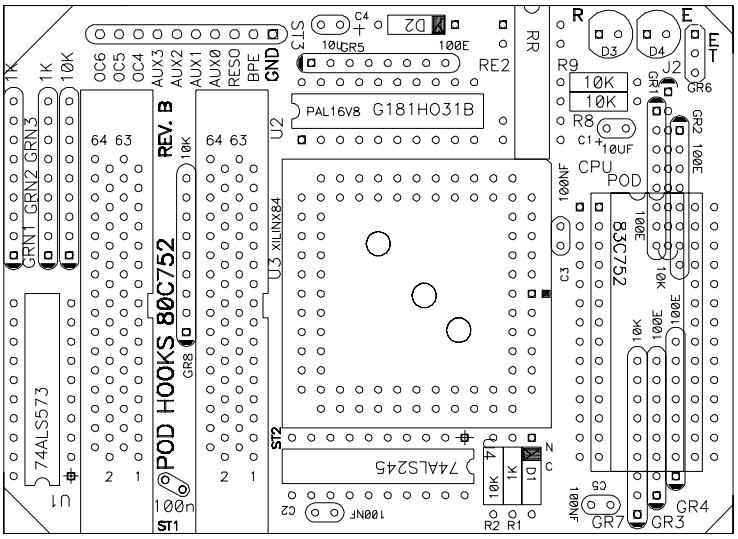
See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

Philips 80752 Hooks POD rev. B

Ordering code	IC81032
POD Speed (MHz)	16
Emulator Speed (ns)	90
Bank switch support	NO
Exchange CPU	NO
Dimensions (mm)	96x70
Pin 1 position (mm)	79x44

See "Intel 8051 Family – Philips Hooks PODs" on page 387.

This POD can be used on iC181, iC1000 and the PowerEmulator unit.



Target POD pinout is a standard DIP28.

Emulated CPU
80C751
80C752

This POD uses a special emulation mode (hooks mode) to emulate the CPU. As a consequence, ports P1 and P3 are emulated with on POD XILINX LCA resulting in slightly different AC and DC characteristics than the original CPU.

Both ports have serial 100-ohm resistors as well as 10k pull-ups.

Note: As clock source a standalone clock must always be used, either internal or external from the target. The Clock signal is not directly connected to the CPU pin because the clock signal is required for HOOKS mode implementation. Thus when external clock is selected, the oscillator must be used in the target and not the crystal which would not oscillate at all since it's not connected directly to the CPU pin.

Vcc source on this POD is configured via J2 jumper:

Source	Position
Emulator	E
Target	T

Jumper J2 Vcc Source settings

Note: Jumpers can only be changed when the Emulator is switched off.

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.

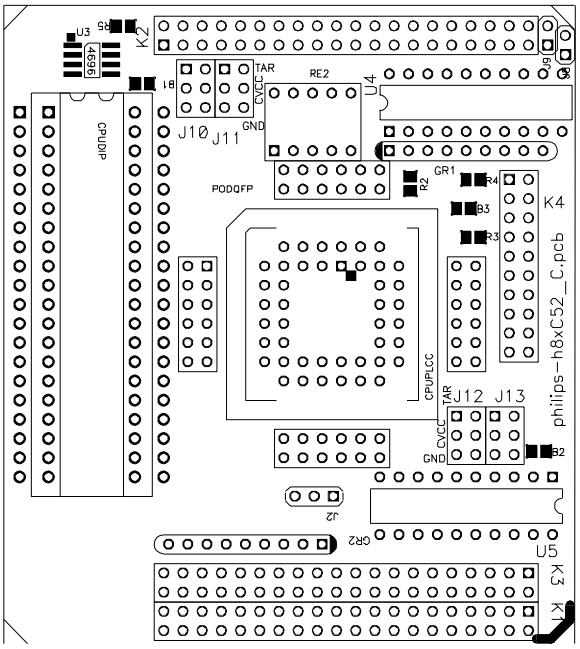
Philips H-8xC52 POD rev. C

Ordering code	IC10020	
POD Speed (MHz) (*)	40	33
Emulator Speed (ns)	65	90
Bank switch support	YES	
Exchange CPU	YES	
Dimensions (mm)	75.5x84.5	
Pin 1 position (mm)	27x50	

Note (*): See the note at the bottom of Emulated CPUs list.

See "Intel 8051 Family – Philips Hooks PODs" on page 387.

This POD can be used on iC1000 and the PowerEmulator unit. This POD can not be used with iC181.



Emulated CPUs
80C51
80C31
8xC52
8xC32
80C52
80C54
80C58
8xC053
8xC054
8xC51 FA, FB, FC
8xC51 RA, RB, RC, RD
8xC51 RA+, RB+, RC+, RD+
89C51 RB2, RC2, RD2 (*)
8xC504
8xC524
8xC528
8xC550
8xC575
8xC591
8xC652
8xC654
AT89Cx051
AT89(C)(S)5x
TS80C81Rx2
TS80C51U2
TS80C32
TS80C31X2

Note (*): When emulating 89C51Rx2 CPUs, the H-89C51Rx2 POD must be selected in the software and the appropriate CPU must be inserted into the POD. The maximum POD speed in this case is 20 MHz, since te Rx2 CPUs require 6 cycles for one machine cycle. In any other case, the H-8xC52 POD must be selected in the software. In this case, the maximum POD speed is 40 MHz, since these CPUs require 12 cycles for one machine cycle.

Jumper J2 selects Emulator V_{CC} level

V_{CC} level	J2 setting
3.3 V	1-2
5.0 V	2-3

Jumper J2 settings

Target POD pinout is DIL40 and T_PLCC44 (See "T_PLCC44 POD Target Pinout" on page 582).

The original 8052 MCU in a PLCC socket has four pins, that are not connected. Some other MCUs use these pins for extra functionallity. Jumpers are available on the POD which allow each of these pins to be connected to either the Target, to VCC or to GND.

Jumper 10 affects the CPU pin 1.

Jumper setting	Pin connected to
1-2	Target pin 1
3-4	VCC
5-6	GND

Jumper J10 setting

Note: Make sure always only one jumper is inserted into either the 1-2, 3-4 or 5-6 setting. Never insert more than one jumper. Otherwise, damage to the POD, the Target or the Emulator can occur.

Jumper 11 affects the CPU pin 12.

Jumper setting	Pin connected to
1-2	Target pin 12
3-4	VCC
5-6	GND

Jumper J11 setting

Note: Make sure always only one jumper is inserted into either the 1-2, 3-4 or 5-6 setting. Never insert more than one jumper. Otherwise, damage to the POD, the Target or the Emulator can occur.

Jumper 12 affects the CPU pin 23.

Jumper setting	Pin connected to
1-2	Target pin 23
3-4	VCC
5-6	GND

Jumper J12 setting

Note: Make sure always only one jumper is inserted into either the 1-2, 3-4 or 5-6 setting. Never insert more than one jumper. Otherwise, damage to the POD, the Target or the Emulator can occur.

Jumper 13 affects the CPU pin 34.

Jumper setting	Pin connected to
1-2	Target pin 34
3-4	VCC
5-6	GND

Jumper J13 setting

Note: Make sure always only one jumper is inserted into either the 1-2, 3-4 or 5-6 setting. Never insert more than one jumper. Otherwise, damage to the POD, the Target or the Emulator can occur.

Jumper J8 (located in the top right corner) selects the level of active RESET.

Jumper setting	Active RESET
Set	Active RESET level is 0
Removed	Active RESET level is 1

Jumper J8 setting

Summary of jumper settings for Philips 8xC591:

Jumper	Jumper setting	Description
J8	Set	Active RESET level is 1
J10	5-6	Pin 1 connected to GND
J11	1-2	Pin 12 connected to Target pin 12
J12	3-4	Pin 23 connected to VCC
J13	1-2	Pin 34 connected to Target pin 34

Summary of jumper settings for other MCUs:

Jumper	Jumper setting	Description
J8	Removed	Active RESET level is 0
J10	1-2	Pin 1 connected to Target pin 1
J11	1-2	Pin 12 connected to Target pin 12
J12	1-2	Pin 23 connected to Target pin 23
J13	1-2	Pin 34 connected to Target pin 34

Note: As clock source a standalone clock must always be used, either internal or external from the target. The Clock signal is not directly connected to the CPU pin because the clock signal is required for HOOKS mode implementation. Thus when external clock is selected, the oscillator must be used in the target and not the crystal which would not oscillate at all since it's not connected directly to the CPU pin.

This POD uses a special emulation mode (hooks mode) to emulate the CPU. As a consequence, ports P0 and P2 are emulated with on POD XILINX CPLD (type XCS20XL) resulting in slightly different AC and DC characteristics to the original CPU.
Both ports and ALE and PSEN lines have serial 100-ohm resistors for protection; P2 has additional 1k pull-ups on the target side.

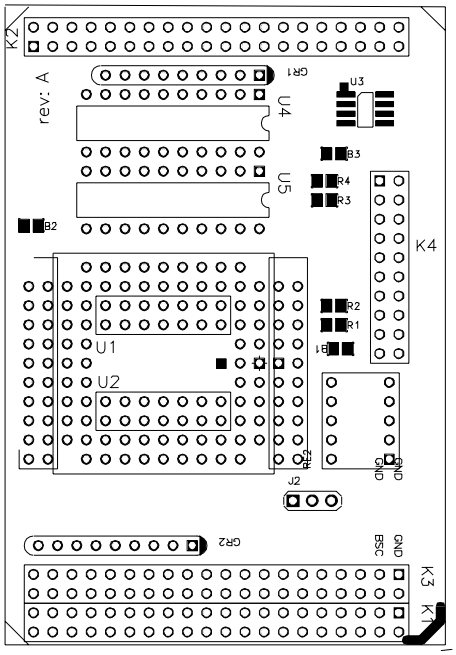
See "In-Circuit Emulation PODs" on page 324 for common K0/ST3 connector signals.

Philips H-8xC554 POD rev. A

Ordering code	IC10021
POD Speed (MHz)	33
Emulator Speed (ns)	90
Bank switch support	YES
Exchange CPU	YES
Dimensions (mm)	58.5x84.5
Pin 1 position (mm)	36x37.5

See "Intel 8051 Family – Philips Hooks PODs" on page 387.

This POD can be used on iC1000 and the PowerEmulator unit. It can not be used with iC181.



Emulated CPU
8xC552
8xC554

Jumper J2 selects Emulator V_{CC} level

V_{CC} level	J2 setting
3.3 V	1-2
5.0 V	2-3

Jumper J2 settings

Target POD pinout is T_PLCC68 (See "T_PLCC68 POD Target Pinout" on page 583)

See "In-Circuit Emulation PODs" on page 324 for common ST3 connector signals.